



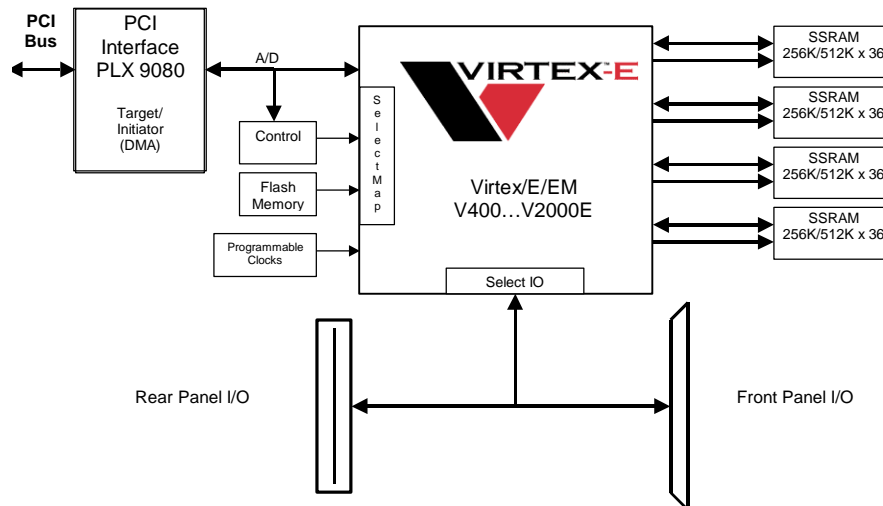
# ADM-XRC

## Xilinx Reconfigurable Computer



### Features

- Industry standard PMC format
- Support for the largest Xilinx Virtex, VirtexE and Virtex-EM FPGA devices
- On board re-programmable flash memory for embedded configuration
- Wide range of IP cores available
- High performance bus mastering PCI interface using PLX9080
- High density I/O connector in standard SCSI-2 format or optional rear panel I/O via Pn4
- Support for Xilinx ChipScope for debugging
- 4 independent banks of 256k/512k x 36 bits of ZBT SRAM
- Programmable clock generator
- Software Development Kits for WinNT, Win2000, Linux and VxWorks





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### Specification

<b>PCI Bus</b>	Adapters available for PCI plug-in, CompactPCI and VME formats Revision 2.1 Compliant 3.3V or 5V I/O Twin DMA channels support data rates of 116Mbytes/sec to Virtex.
<b>Flash</b>	2 Mbyte User programmable
<b>FPGA</b>	All Xilinx Virtex, Virtex-E and Virtex-EM BGA 560 devices
<b>SRAM</b>	Standard 100 pin TQFP ZBT SSRAM. 4 banks x 256k x 36 4 banks x 512k x 36 optional
<b>Configuration</b>	PCI Bus direct to SelectMAP port for fast configuration Flash boot on power up External JTAG connector
<b>SelectMap</b>	Configuration port supports direct access to Virtex configuration for download or readback. DMA can be used to configure at up to 30Mbytes/sec
<b>JTAG</b>	A standard JTAG port is provided that can be used for programming both the Virtex FPGA and CPLD support logic for debugging or firmware upgrade
<b>Clocks</b>	On board clock generator provides a synchronous local bus clock for the PCI interface and the Virtex FPGA. A second clock is provided to the Virtex FPGA for user applications and can be free running or stepped under software control. Both clocks are programmable and can be used by the Virtex Clock DLL functions:- <b>Local Bus</b> 400kHz to 40 MHz <b>User Clock</b> 0Hz to 100 MHz
<b>External I/O</b>	Front Panel 34 I/O lines from FPGA Bank Rear Panel 53 I/O lines from FPGA Bank optional

### Ordering Information

ADM-XRC/xxx-y/z  
xxx - Virtex size  
y - Virtex speed  
z - Memory 4(MB) or 8(MB)