ALPHA DATA

ADC-VPX3-XMC User Manual

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Table Of Contents

Tables

Figures

1 About the Hardware

The ADC-VPX3-XMC is an Open VPX compliant XMC carrier designed to host Alpha Data ADM-XRC series of FPGA mezzanine cards.

The ADC-VPX3-XMC is compatible with PCIe Gen3 and lower.

This carrier supports ADM-XRC series cards utilizing Virtex 6 and newer FPGAs.

The ADC-VPX3-XMC also supports the optional P4 auxiliary IO connector available on most Alpha Data mezzanine cards.

Two full size mSATA sites offer massive SSD storage options.

Open VPX Compliance List

- SLT3-PAY-2F2U-14.2.3
- SLT3-PAY-1F1F2U-14.2.4
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-2F-14.2.7
- SLT3-PAY-1F4U-14.2.8
- SLT3-PAY-8U-14.2.9
- SLT3-PER-2F-14.3.1
- SLT3-PER-1F-14.3.2
- SLT3-PER-1U-14.3.3
- SLT3-STO-2U-14.5.1

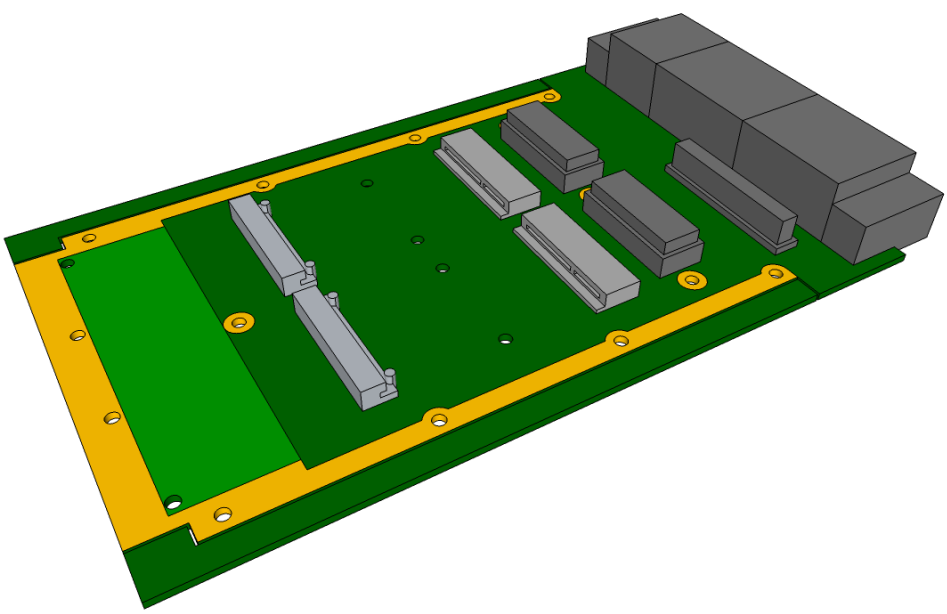

Figure 1: ADC-VPX3-XMC Photo

1.1 Architecture

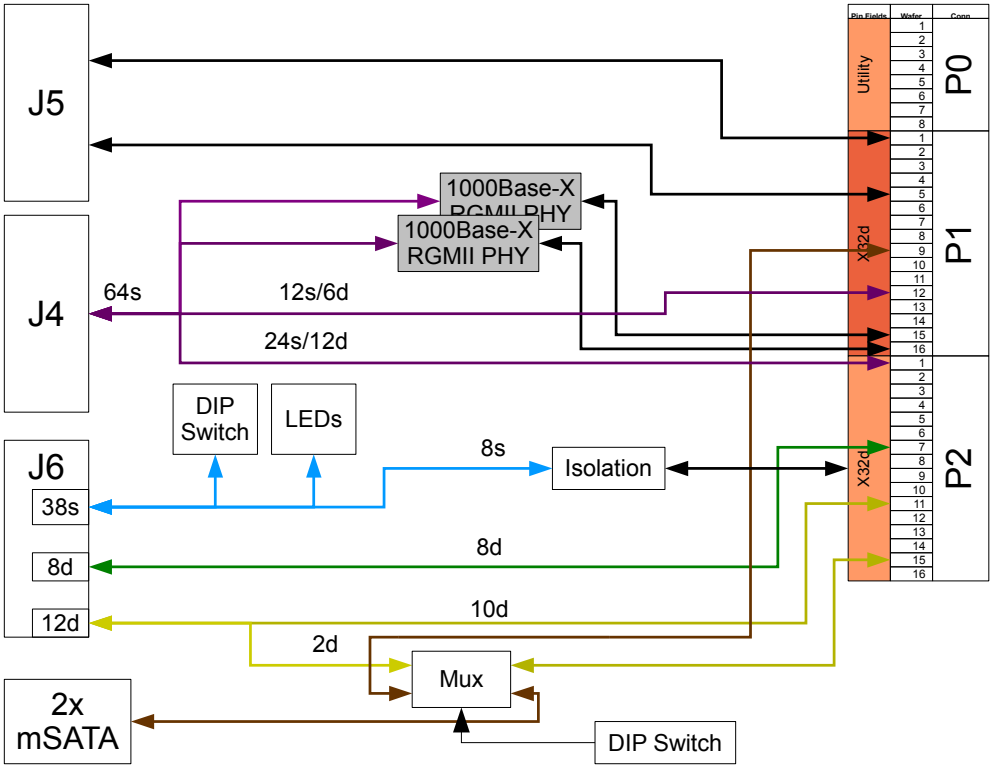

Figure 2: ADC-PCIE-XMC Block Diagram

1.2 Board Features

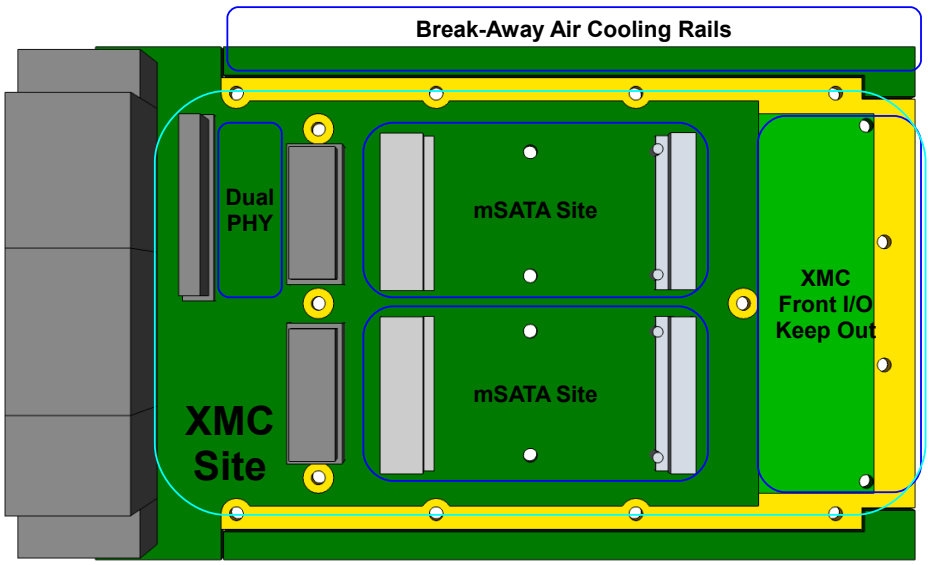

Figure 3: Top Side Features

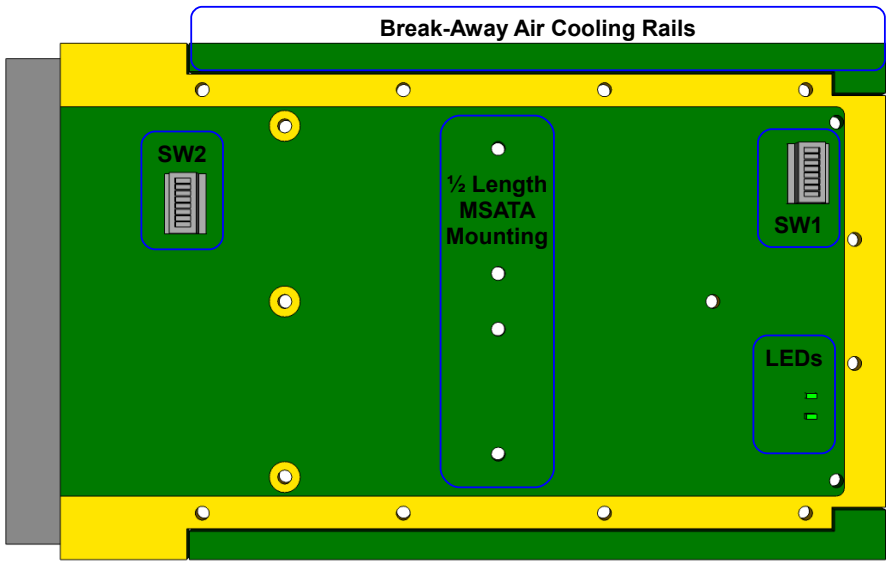

Figure 4: Bottom Side Features

1.2.1 DIP Switches

The ADC-PCIE-XMC has two 8 position DIP switches which control the following functions.

SW1 Controls critical board features and is used for generic user input to the FPGA on the mezzanine module.

Switch Index	Function	Off Position	On Position
1	SATA Mux	mSATA Routed to J6	mSATA Routed to P1
2	PHY RGMII Voltage	7 Series Devices	Virtex 6
3	mSATA 1.5V Supply Enable 1	ON	OFF
4	mSATA 1.5V Supply Enable 2	ON	OFF
5	User_Select1	1	0
6	User_Select2	1	0
7	User_Select3	1	0
8	User_Select4	1	0

Table 1: Control Switch (SW1)

SW2 is used to isolate the 8 optional user defined IO on P2 Wafer G.

Switch Index	Function	Off Position	On Position
1	SE1_VPX(P2.G1)	Isolated	Connected
2	SE2_VPX(P2.G3)	Isolated	Connected
3	SE3_VPX(P2.G5)	Isolated	Connected
4	SE4_VPX(P2.G7)	Isolated	Connected
5	SE5_VPX(P2.G9)	Isolated	Connected
6	SE6_VPX(P2.G11)	Isolated	Connected
7	SE7_VPX(P2.G13)	Isolated	Connected
8	SE8_VPX(P2.G15)	Isolated	Connected

Table 2: Isolation Switch (SW2)

1.2.2 LEDs

Four status LEDs display system and user defined status. The user defined status LEDs are connected through a buffer to the target FPGA on the mezzanine module.

LED	Color	Control Signal/Function
D1	GREEN	System OK
D2	RED	System Fault
D3	GREEN	USER_LED1
D4	RED	USER_LED2

Table 3: LEDs

1.2.3 mSATA Sites

The ADC-VPX3-XMC can host two mSATA Solid State Drives. Access to these drives can be muxed between the VPX backplane and the FPGA mezzanine card (see **Section 1.2.1, "DIP Switches"**). The connection to the VPX backplane on P1 is compliant to the Storage Modules defined in OpenVPX (SLT3-STO-2U-14.5.1)

1.2.4 Dual PHY

A Dual PHY is used to convert the two 1000Base-X signals on wafers 15 and 16 of P1 to RGMII. The RGMII signals are then routed to the GPIO of the Target FPGA on the mezzanine module. An MDIO interface is available for debugging and control.

> **Note:** SW1-2 MUST match the mezzanine card installed in the carrier. Incorrect switch position will kill the RGMII interface and possibly damage the PHY.

1.2.5 Clocking

1.2.5.1 PCIe REFCLK

An on-board PCIe REFCLK generator supplies the XMC site with the necessary PCIe REFCLK.

1.2.5.2 AUXCLK

The ADC-VPX3-XMC forwards the AUXCLK signal from P0 through J4. While AUXCLK is connected to the Target FPGA of the mezzanine card, it is not guaranteed to be on clock capable IO pins.

1.2.6 Cooling Option

The ADC-VPX3-XMC is designed to fully accommodate both air cooled and conduction cooled chassis both with and without front IO.

1.2.6.1 Air Cooled

Two removable tabs along the sides of board allow for easy insertion into standard air cooled chassis. With extremely low power consumption this Carrier does not require any heatsinks in the air cooled configuration.

The removable tabs can be replaced by metal tabs if a customer requires a board that can be both air cooled and conuduction cooled.

1.2.6.2 Conduction Cooled

A Vita 48.2 compliant conduction cooled frame will ship with the board for conduction cooled applications. All Alpha Data XMCs have conduction cooled options that are compliant with this carrier.

The heat frame for this board contains a removable front bar. With the front bar removed, Alpha Data front panel XRM modules can be used in conduction cooling application.

Custom conduction cooling assemblies can be designed to optimize heat transfer from critical components to the side rails as needed. Please contact sales@alpha-data.com for details.

1.2.7 VPX Mechanical Keying

The ADC-VPX3-XMC is delivered with the VPX guides unkeyed. For custom keying options please contact sales@alpha-data.com.

2 Rear Transition Module (RTM)

The ADC-VPX3-XMC-RTM is a Rear Transition module that breaks out all signals from the ADC-VPX3-XMC to be used in development environments.

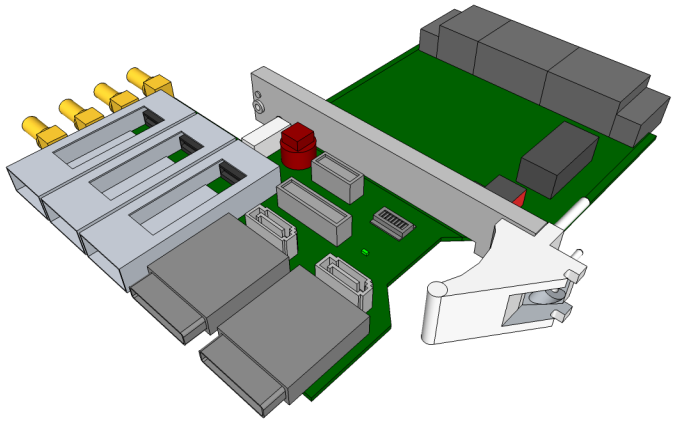

Figure 5: ADC-VPX3-XMC Photo

2.1 Architecture

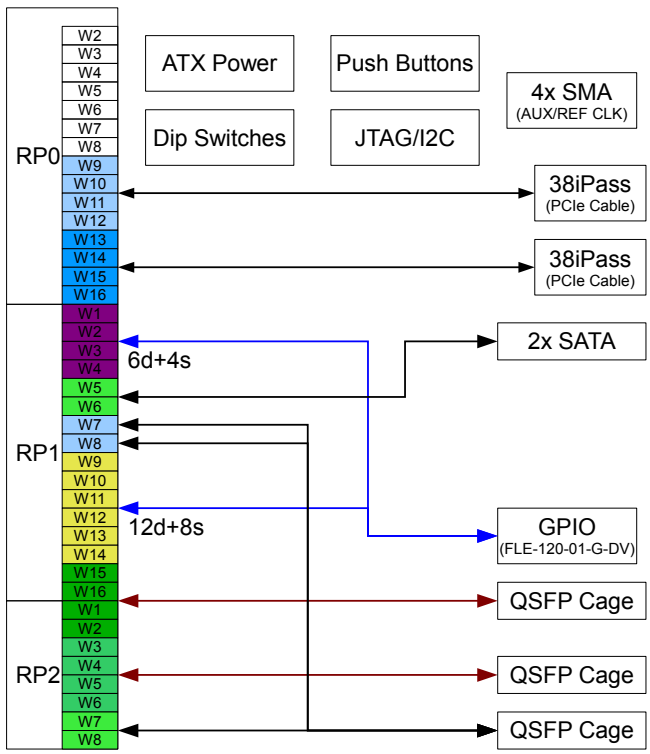

Figure 6: ADC-PCIE-XMC Block Diagram

2.2 Board Features

2.2.1 RTM DIP Switch

The ADC-PCIE-XMC-RTM has a single 8 position DIP switch which controls the following functions.

Switch Index	Function	Off Position	On Position
1	Non Volatile Memory Read-Only	Memory Read-Only	Memory Read-Write
2	Reserved	No Connect	No Connect
3	GA0	1	0
4	GA1	1	0
5	GA2	1	0
6	GA3	1	0
7	GA4	1	0
8	GAP	1	0

Table 4: RTM Switch (SW1)

2.2.2 SATA Connectors

The RTM contains two Vertical SATA receptacles that connect to the mSATA sites on the carrier board.

2.2.3 QSFP Cages

Three QSFP cages break out all user defined High Speed Serial IO (HSSIO) and the two control lanes on P1 Wafers 15 and 16.

Numerous copper and optical cabling breakout solutions exist from multiple suppliers for QSFP cable assemblies.

2.2.4 AUXCLK

The ADC-VPX3-XMC-RTM has two SMA jacks for the AUXCLK signal. The RTM does not perform any signal condition to the AUXCLK signal, which must be LVDS for proper FPGA operation. Ensure the AUXCLK is LVDS before it reaches the RTM.

2.2.5 iPass PCIe Cabling

Two x4 PCIe External Cable jacks are available on the RTM. The endpoints are compliant with PCI Express® External Cabling Specification Revision 1.0 and do not support the optional 3.3V power delivery scheme.

Desktop to cable adapters can be purchased from third party suppliers to assist with development using desktop PCs.

2.2.6 JTAG

The ADC-VPX3-XMC-RTM has a 14-pin parallel cable JTAG receptacle compatible with Xilinx programming cables.

2.2.7 GPIO

Two socket strips break out the GPIO signals from the backplane. J19 is the smaller of the two and breaks out the single ended only signals (Samtec p/n FLE-113-01-G-DV). J20 is larger and breaks out the 19 differential pairs from the backplane (Samtec p/n FLE-120-01-G-DV).

Mating cable assemblies can be found at www.samtec.com

2.2.8 System Reset

SW2 is a momentary push-button switch that will trigger a system wide reset.

2.2.9 ATX Power Supply

An ATX power supply jack is located near the VPX backplane. This is intended for use in standalone operation outside of a chassis.

After an ATX power supply is plugged in and turned on, SW3 provides the PS_ON_L signal to deliver power to the system.

2.2.10 I2C

J3 provides access to the system SDA and SCL lines.

3 Carrier Connector Pin Assignments

3.1 P1

The following table shows the connectivity through P1 when the mSATA sites are driven from the backplane.

Signal	Carrier Connector.Pin	P1 Pin	RP0/RP1.Pin	RTM Connector.Pin
PCIE_RX0_P	J5.A11	A1	RP0.A9	J21.B2
PCIE_RX0_N	J5.B11	B1	RP0.B9	J21.B3
PCIE_TX0_P	J5.A1	D1	RP0.D9	J21.A2
PCIE_TX0_N	J5.B1	E1	RP0.E9	J21.A3
PCIE_RX1_P	J5.D11	B2	RP0.B10	J21.B5
PCIE_RX1_N	J5.E11	C2	RP0.C10	J21.B6
PCIE_TX1_P	J5.D1	E2	RP0.E10	J21.A5
PCIE_TX1_N	J5.E1	F2	RP0.F10	J21.A6
PCIE_RX2_P	J5.A13	A3	RP0.A11	J21.B8
PCIE_RX2_N	J5.B13	B3	RP0.B11	J21.B9
PCIE_TX2_P	J5.D13	D3	RP0.D11	J21.A8
PCIE_TX2_N	J5.E13	E3	RP0.E11	J21.A9
PCIE_RX3_P	J5.A3	B4	RP0.B12	J21.B11
PCIE_RX3_N	J5.B3	C4	RP0.C12	J21.B12
PCIE_TX3_P	J5.D3	E4	RP0.E12	J21.A11
PCIE_TX3_N	J5.E3	F4	RP0.F12	J21.A12
PCIE_RX4_P	J5.A15	A5	RP0.A13	J22.B2
PCIE_RX4_N	J5.B15	B5	RP0.B13	J22.B3
PCIE_TX4_P	J5.D15	D5	RP0.D13	J22.A2
PCIE_TX4_N	J5.E15	E5	RP0.E13	J22.A3
PCIE_RX5_P	J5.A5	B6	RP0.B14	J22.B5
PCIE_RX5_N	J5.B5	C6	RP0.C14	J22.B6
PCIE_TX5_P	J5.D5	E6	RP0.E14	J22.A5
PCIE_TX5_N	J5.E5	F6	RP0.F14	J22.A6
PCIE_RX6_P	J5.A17	A7	RP0.A15	J22.B8
PCIE_RX6_N	J5.B17	B7	RP0.B15	J22.B9
PCIE_TX6_P	J5.D17	D7	RP0.D15	J22.A8
PCIE_TX6_N	J5.E17	E7	RP0.E15	J22.A9
PCIE_RX7_P	J5.A7	B8	RP0.B16	J22.B11
PCIE_RX7_N	J5.B7	C8	RP0.C16	J22.B12
PCIE_TX7_P	J5.D7	E8	RP0.E16	J22.A11
PCIE_TX7_N	J5.E7	F8	RP0.F16	J22.A12
STRupt1-R_P	J1.33	A9	RP1.A1	J17.2
STRupt1-R_N	J1.31	B9	RP1.B1	J17.3
STRupt1-T_P	J1.23	D9	RP1.D1	J17.6

Table 5: P1 (continued on next page)

Signal	Carrier Connector.Pin	P1 Pin	RP0/RP1.Pin	RTM Connector.Pin
STRupt1-T_N	J1.25	E9	RP1.E1	J17.5
STRupt2-R_P	J2.33	B10	RP2.B2	J18.2
STRupt2-R_N	J2.31	C10	RP1.C2	J18.3
STRupt2-T_P	J2.23	E10	RP1.E2	J18.6
STRupt2-T_N	J2.25	F10	RP1.F2	J18.5
GP18_P	J4.62	A11	RP1.A3	J20.37
GP18_N	J4.64	B11	RP1.B3	J20.38
GP17_P	J4.61	D11	RP1.D3	J20.35
GP17_N	J4.63	E11	RP1.E3	J20.36
GP16_P	J4.58	B12	RP1.B4	J20.33
GP16_N	J4.60	C12	RP1.C4	J20.34
GP15_P	J4.57	E12	RP1.E4	J20.31
GP15_N	J4.59	F12	RP1.F4	J20.32
GP14_P	J4.54	A13	RP1.A5	J20.29
GP14_N	J4.56	B13	RP1.B5	J20.30
GP13_P	J4.53	D13	RP1.D5	J20.27
GP13_N	J4.55	E13	RP1.E5	J20.28
SE12	J6.F5	C14	RP1.C6	J19.16
SE11	J6.C5	B14	RP1.B6	J19.15
SE10	J6.F6	F14	RP1.F6	J19.12
SE9	J6.C6	E14	RP1.E6	J19.11
ETH2_RX_P	U10.1	A15	RP1.A7	J14.25
ETH2_RX_N	U10.2	B15	RP1.B7	J14.24
ETH2_TX_P	U10.4	D15	RP1.D7	J14.6
ETH2_TX_N	U10.5	E15	RP1.E7	J14.5
ETH1_RX_P	U9.1	B16	RP1.B8	J14.14
ETH1_RX_N	U9.2	C16	RP1.C8	J14.15
ETH1_TX_P	U9.4	E16	RP1.E8	J14.33
ETH1_TX_N	U9.5	F16	RP1.F8	J14.34

Table 5: P1

3.2 P2

The following table shows the connectivity through P2 when the mSATA sites are driven from the backplane.

Note: The ADC-VPX3-XMC is an OpenVPX compliant carrier. Due to inconsistancies in different VITA specifications, this carrier uses the signal polarity map present in Vita 65 table 6.3.1 (OpenVPX). If the host system requires VITA 46.9 polarity mapping, the user must invert the polarity of these differential signals internal to the FPGA.

Signal Name	Carrier Connector.Pin	P2 Pin	RP1/RP2.Pin	RTM Connector.Pin
SE1	J6.C10	G1	RP1.G9	J19.3
SE2	J6.F10	G3	RP1.G11	J19.4
SE3	J6.C9	G5	RP1.G13	J19.5
SE4	J6.F9	G7	RP1.G15	J19.6
SE5	J6.C8	G9	RP2G.1	J19.7
SE6	J6.F8	G11	RP2.G3	J19.8
SE7	J6.C7	G13	RP2.G5	J19.9
SE8	J6.F7	G15	RP2.G7	J19.10
GP12_P	J4.52	A1	RP1.A9	J20.25
GP12_N	J4.50	B1	RP1.B9	J20.26
GP11_P	J4.51	D1	RP1.D9	J20.23
GP11_N	J4.49	E1	RP1.E9	J20.24
GP10_P	J4.48	B2	RP1.B10	J20.21
GP10_N	J4.46	C2	RP1.C10	J20.22
GP9_P	J4.47	E2	RP1.E10	J20.19
GP9_N	J4.45	F2	RP1.F10	J20.20
GP8_P	J4.44	A3	RP1.A11	J20.17
GP8_N	J4.42	B3	RP1.B11	J20.18
GP7_P	J4.43	D3	RP1.D11	J20.15
GP7_N	J4.41	E3	RP1.E11	J20.16
GP6_P	J4.40	B4	RP1.B12	J20.13
GP6_N	J4.38	C4	RP1.C12	J20.14
GP5_P	J4.39	E4	RP1.E12	J20.11
GP5_N	J4.37	F4	RP1.F12	J20.12
GP4_P	J4.36	A5	RP1.A13	J20.9
GP4_N	J4.34	B5	RP1.B13	J20.10
GP3_P	J4.35	D5	RP1.D13	J20.7
GP3_N	J4.33	E5	RP1.E13	J20.8
GP2_P	J4.32	B6	RP1.B14	J20.5
GP2_N	J4.30	C6	RP1.C14	J20.6
GP1_P	J4.31	E6	RP1.E14	J20.3
GP1_N	J4.29	F6	RP1.F14	J20.4
P2_RX0_P	J6.A11	A7	RP1.A15	J12.17

Table 6: P2 (continued on next page)

Signal Name	Carrier Connector.Pin	P2 Pin	RP1/RP2.Pin	RTM Connector.Pin
P2_RX0_N	J6.B11	B7	RP1.B15	J12.18
P2_TX0_P	J6.A1	D7	RP1.D15	J12.36
P2_TX0_N	J6.B1	E7	RP1.E15	J12.37
P2_RX1_P	J6.D11	B8	RP1.B16	J12.22
P2_RX1_N	J6.E11	C8	RP1.C16	J12.21
P2_TX1_P	J6.D1	E8	RP1.E16	J12.3
P2_TX1_N	J6.E1	F8	RP1.F16	J12.2
P2_RX2_P	J6.A13	A9	RP2.A1	J12.14
P2_RX2_N	J6.B13	B9	RP2.B1	J12.15
P2_TX2_P	J6.A3	D9	RP2.D1	J12.33
P2_TX2_N	J6.B3	E9	RP2.E1	J12.34
P2_RX3_P	J6.D13	B10	RP2.B2	J12.25
P2_RX3_N	J6.E13	C10	RP2.C2	J12.24
P2_TX3_P	J6.D3	E10	RP2.E2	J12.6
P2_TX3_N	J6.E3	F10	RP2.F2	J12.5
P2_RX4_P	J6.A15	A11	RP2.A3	J13.17
P2_RX4_N	J6.B15	B11	RP2.B3	J13.18
P2_TX4_P	J6.A5	D11	RP2.D3	J13.36
P2_TX4_N	J6.B5	E11	RP2.E3	J13.37
P2_RX5_P	J6.D15	B12	RP2.B4	J13.22
P2_RX5_N	J6.E15	C12	RP2.C4	J13.21
P2_TX5_P	J6.D5	E12	RP2.E4	J13.3
P2_TX5_N	J6.E5	F12	RP2.F4	J13.2
P2_RX6_P	J6.A17	A13	RP2.A5	J13.14
P2_RX6_N	J6.B17	B13	RP2.B5	J13.15
P2_TX6_P	J6.A7	D13	RP2.D5	J13.33
P2_TX6_N	J6.B7	E13	RP2.E5	J13.34
P2_RX7_P	J6.D17	B14	RP2.B6	J13.25
P2_RX7_N	J6.E17	C14	RP2.C6	J13.24
P2_TX7_P	J6.D7	E14	RP2.E6	J13.6
P2_TX7_N	J6.E7	F14	RP2.F6	J13.5
P2_RX8_P	J6.A19	A15	RP2.A7	J14.17
P2_RX8_N	J6.B19	B15	RP2.B7	J14.18
P2_TX8_P	J6.A9	D15	RP2.D7	J14.36
P2_TX8_N	J6.B9	E15	RP2.E7	J14.37
P2_RX9_P	J6.D19	B16	RP2.B8	J14.22
P2_RX9_N	J6.E19	C16	RP2.C8	J14.21
P2_TX9_P	J6.D9	E16	RP2.E8	J14.3
P2_TX9_N	J6.E9	F16	RP2.F8	J14.2

Table 6: P2

3.3 mSATA (SSD) Mux

The following tables show the connectivity changes to P1 and P2 when the mSATA sites are driven from the XMC site.

Signal	Carrier Connector.Pin	P1 Pin	RP0/RP1.Pin	RTM Connector.Pin
STRupt1-R_P	NC	P1.A9	RP1.A1	J17.2
STRupt1-R_N	NC	P1.B9	RP1.B1	J17.3
STRupt1-T_P	NC	P1.D9	RP1.D1	J17.6
STRupt1-T_N	NC	P1.E9	RP1.E1	J17.5
STRupt2-R_P	NC	P1.B10	RP2.B2	J18.2
STRupt2-R_N	NC	P1.C10	RP1.C2	J18.3
STRupt2-T_P	NC	P1.E10	RP1.E2	J18.6
STRupt2-T_N	NC	P1.F10	RP1.F2	J18.5
P2_RX0_P	NC	A7	RP1.A15	J12.17
P2_RX0_N	NC	B7	RP1.B15	J12.18
P2_TX0_P	NC	D7	RP1.D15	J12.36
P2_TX0_N	NC	E7	RP1.E15	J12.37
P2_RX1_P	NC	B8	RP1.B16	J12.22
P2_RX1_N	NC	C8	RP1.C16	J12.21
P2_TX1_P	NC	E8	RP1.E16	J12.3
P2_TX1_N	NC	F8	RP1.F16	J12.2

Table 7: Modifications to P1 and P2

Signal	Carrier Connector.Pin	Carrier Connector.Pin
STRupt1-R_P	J1.33	J6.A1
STRupt1-R_N	J1.31	J6.B1
STRupt1-T_P	J1.23	J6.A11
STRupt1-T_N	J1.25	J6.B11
STRupt2-R_P	J2.33	J6.D1
STRupt2-R_N	J2.31	J6.E1
STRupt2-T_P	J2.23	J6.D11
STRupt2-T_N	J2.25	J6.E11

Table 8: New mSATA Site Connectivity to J6

3.4 Debug Signals

The following table shows the connectivity between the XMC site and the user defined switches, LEDS, and extra mSATA peripheral signals.

Signal	Carrier Connector.Pin	Origin
USER_LED1	J6.C1	D3
USER_LED2	J6.F1	D4
USER_SEL1	J6.C3	SW1-5
USER_SEL2	J6.F3	SW1-6
USER_SEL3	J6.C2	SW1-7
USER_SEL4	J6.F2	SW1-8
SATA1_PRSNT_L	J6.C4	J1
SATA2_PRSNT_L	J6.F4	J2

Table 9: Debug Signals

3.5 Two Wire Interfaces

Multiple 4 pin headers are used for debugging access to the different two wire data interfaces on the ADC-VPX3-XMC and ADC-VPX3-XMC-RTM. All connectors use the same pin assignment.

Signal	Header Pin
VDD_REF	1
GND	2
DATA	3
CLOCK	4

Table 10: Two Wire Header Signals

The following table details the different two wire interface headers and their associated endpoints.

Header	Function
Carrier J7	MDIO Interface to Ethernet PHY
RTM J3	I2C System Interface
RTM J8	I2C to QSFP J12
RTM J15	I2C to QSFP J13
RTM J16	I2C to QSFP J14

Table 11: Two WIre Header Descriptions

3.6 RTM GPIO Connectors

Signal	J19 Pin		J19 Pin	Signal
GND	1	|	2	GND
SE1	3	|	4	SE2
SE3	5	|	6	SE4
SE5	7	|	8	SE6
SE7	9	|	10	SE8
SE9	11	|	12	SE10
GND	13	|	14	GND
SE11	15	|	16	SE12
NC	17	|	18	NC
NC	19	|	20	NC
NC	21	|	22	NC
NC	23	|	24	NC
GND	25	|	26	GND

Table 12: J19

Signal	J20 Pin		J20 Pin	Signal
GND	1	|	2	GND
GP1_P	3	|	4	GP1_N
GP2_P	5	|	6	GP2_N
GP3_P	7	|	8	GP3_N
GP4_P	9	|	10	GP4_N
GP5_P	11	|	12	GP5_N
GP6_P	13	|	14	GP6_N
GP7_P	15	|	16	GP7_N
GP8_P	17	|	18	GP8_N
GP9_P	19	|	20	GP9_N
GP10_P	21	|	22	GP10_N
GP11_P	23	|	24	GP11_N
GP12_P	25	|	26	GP12_N
GP13_P	27	|	28	GP13_N
GP14_P	29	|	30	GP14_N
GP15_P	31	|	32	GP15_N
GP16_P	33	|	34	GP16_N
GP17_P	35	|	36	GP17_N
GP18_P	37	|	38	GP18_N
GND	39	|	40	GND

Table 13: J20

Revision History:

Date	Revision	Changed By	Nature of Change
25 Sep 2012	0.1	K. Roth	Preliminary

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