ALPHA DATA

FMC-CLINK-MINI User Manual

Revision: V1.1

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1 Introduction

The FMC-CLINK-MINI is a VITA 57.1 compliant Single Width LPC FMC module, designed for use with Alpha Data's VITA 57.1 compliant carrier cards. It provides the user with the connectivity to implement computationally intensive applications such as frame grabbers, digital video communications and image processing systems in FPGA fabric.

The adapter provides the connection between the FPGA card and the industry standard **CameraLink** high-speed digital camera interface using the standard **Shrunk Delta Ribbon Connectors** from 3M.

The FMC-CLINK-MINI provides support for 2 **Base** configuration inputs or one **Medium** or **Full** configuration input. In addition to being able to be used for image capture, the FMC-CLINK-MINI may also be used for emulation of either up to two Base format cameras or one Medium / Full format camera.

The FMC also provides four LEDs for use as status indicators, and a RS232 buffer.

For **Power Over Camera Link (PoCL)** support please contact sales@alpha-data.com.

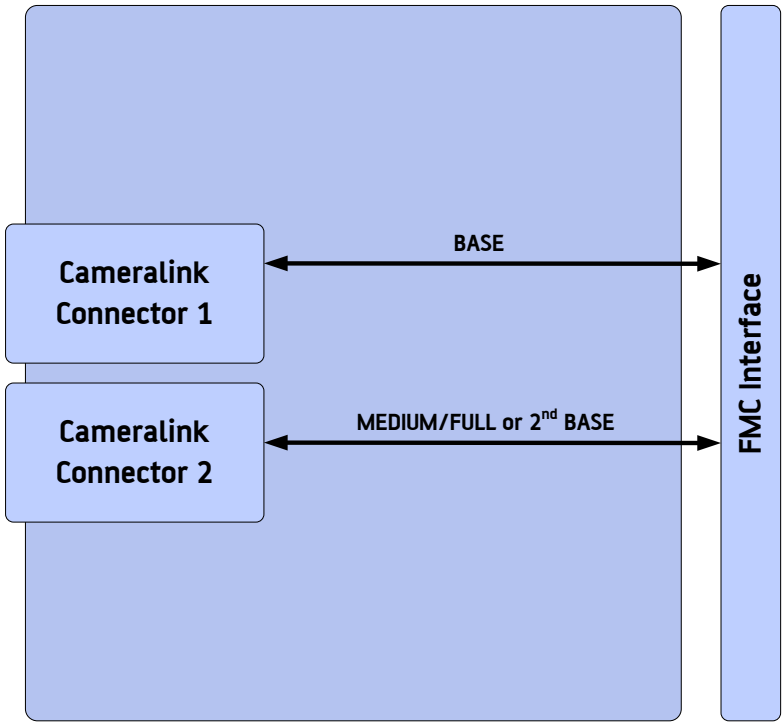

Figure 1 : FMC-CLINK-MINI Block Diagram

1.1 References

Camera Link Specification v1.1 (Automated Imaging Association).

ANSI/VITA 57.1, FPGA Mezzanine Card (FMC) Standard, 2010, ISBN 1-885731-49-3

2 Specification

2.1 Connectors

SDR connector 3M; part number 12226-8250-00FR

2.2 Mating Cableform

SDR cable assembly 3M part number 1SF26-L120-00C-XXX,

where XXX= length in centimetres.

SDR to MDR cable assembly 3M part number 1MF26-L560-00C-XXX, where XXX= length in centimetres.

2.3 Features

Feature of the FMC-CLINK-MINI are shown below.

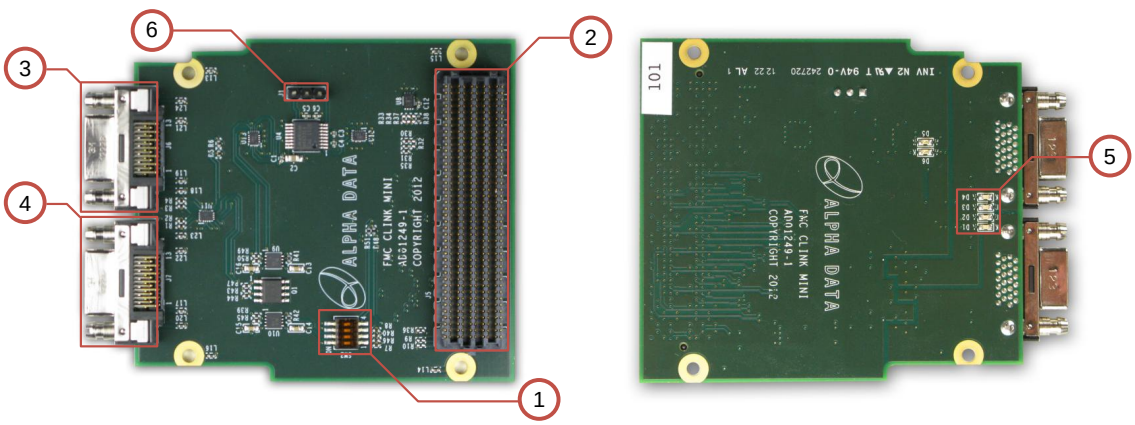

Figure 2 : FMC-CLINK-MINI

Feature	Description
1	Configuration Switch
2	FMC Connector
3	Camera Link Connector 1
4	Camera Link Connector 2
5	LEDs
6	RS232 Header

Table 1 : FMC-CLINK-MINI board features

3 Installation

The FMC-CLINK-MINI is designed to plug in to the FMC front panel connector on a compatible carrier. The retaining screws should be tightened to secure the FMC.

Note: This operation should not be performed while the host PMC, XMC or PCI(e) card is powered up.

3.1 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.

Avoid flexing the board.

3.2 IO Voltage Selection

The required IO voltage for the FMC is 1.8V. This is stored in a ROM on the FMC, as per VITA 57.1 for automatic configuration of supplies.

3.3 Configuration

Before connecting to camera and power up in a system SW1 must be configured appropriately for the application.

Switch	1	2	3	4
Dual Base Input or Output	0	0	0	0
Base/Medium/Full Input or Output	0	0	1	1

Table 2 : Configuration Switch Settings

4 Order Code

FMC-CLINK-MINI.

For further information please contact Alpha Data.

5 Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card when purchased with a compatible Alpha Data FPGA card.

Available applications include a PCIe Camera Link Frame Grabber, and a PCIe Camera Link Emulator compatible with the ADPE-XRC-6T(-L). For more information please contact sales@alpha-data.com

IP Cores for Camera Link serialisation and de-serialisation are also available as a separate purchase to customers purchasing the FMC-CLINK-MINI as a standalone product.

6 Pinout

6.1 Camera Link Pinout

Note:
Some FMC pin have the N/P pairs swapped for particular configurations (signals marked with '*' in the tables below). These signals will need re-inverting in the connected FPGA.

6.1.1 Dual Base Input Configuration

Signal Name	Direction	FMC pin	SDR pin (Con. 1)
xclk_p	in	LA_P_00	9
xclk_n	in	LA_N_00	22
x_p<0>	in	LA_P_02	12
x_n<0>	in	LA_N_02	25
x_p<1>	in	LA_P_03	11
x_n<1>	in	LA_N_03	24
x_p<2>	in	LA_P_04	10
x_n<2>	in	LA_N_04	23
x_p<3>	in	LA_P_05	8
x_n<3>	in	LA_N_05	21
cc_p<1>	out	LA_P_18	5
cc_n<1>	out	LA_N_18	18
cc_p<2>	out	LA_P_19	17
cc_n<2>	out	LA_N_19	4
cc_p<3>	out	LA_P_20	3
cc_n<3>	out	LA_N_20	16
cc_p<4>	out	LA_P_21	15
cc_n<4>	out	LA_N_21	2
ser_tfg_p	in	LA_P_14	6
ser_tfg_n	in	LA_N_14	19
ser_tc_p	out	LA_P_15	20
ser_tc_n	out	LA_N_15	7

Table 3 : Camera Link Connector 1 (Dual Base Input Configuration)

Signal Name	Direction	FMC pin	SDR pin (Con. 2)
xclk_p	in	LA_P_01	9
xclk_n	in	LA_N_01	22
x_p<0>	in	LA_P_06	12
x_n<0>	in	LA_N_06	25
x_p<1>	in	LA_P_07	11
x_n<1>	in	LA_N_07	24
x_p<2>	in	LA_P_08	10
x_n<2>	in	LA_N_08	23
x_p<3>	in	LA_P_09	8
x_n<3>	in	LA_N_09	21
cc_p<1>	out	LA_P_11	5
cc_n<1>	out	LA_N_11	18
cc_p<2>	out	LA_N_12*	17
cc_n<2>	out	LA_P_12*	4
cc_p<3>	out	LA_P_17	3
cc_n<3>	out	LA_N_17	16
cc_p<4>	out	LA_N_13*	15
cc_n<4>	out	LA_P_13*	2
ser_tfg_p	in	LA_P_10	6
ser_tfg_n	in	LA_N_10	19
ser_tc_p	out	LA_P_16	20
ser_tc_n	out	LA_N_16	7

Table 4 : Camera Link Connector 2 (Dual Base Input Configuration)

6.1.2 Base/Medium/Full Input Configuration

Signal Name	Direction	FMC pin	SDR pin (Con. 1)
xclk_p	in	LA_P_00	9
xclk_n	in	LA_N_00	22
x_p<0>	in	LA_P_02	12
x_n<0>	in	LA_N_02	25
x_p<1>	in	LA_P_03	11
x_n<1>	in	LA_N_03	24
x_p<2>	in	LA_P_04	10
x_n<2>	in	LA_N_04	23
x_p<3>	in	LA_P_05	8
x_n<3>	in	LA_N_05	21
cc_p<1>	out	LA_P_18	5
cc_n<1>	out	LA_N_18	18
cc_p<2>	out	LA_P_19	17
cc_n<2>	out	LA_N_19	4
cc_p<3>	out	LA_P_20	3
cc_n<3>	out	LA_N_20	16
cc_p<4>	out	LA_P_21	15
cc_n<4>	out	LA_N_21	2
ser_tfg_p	in	LA_P_14	6
ser_tfg_n	in	LA_N_14	19
ser_tc_p	out	LA_P_15	20
ser_tc_n	out	LA_N_15	7

Table 5 : Camera Link Connector 1 (Base/Medium/Full Input Configuration)

Signal Name	Direction	FMC pin	SDR pin (Con. 2)
yclk_p	in	LA_P_01	9
yclk_n	in	LA_N_01	22
y_p<0>	in	LA_P_06	12
y_n<0>	in	LA_N_06	25
y_p<1>	in	LA_P_07	11
y_n<1>	in	LA_N_07	24
y_p<2>	in	LA_P_08	10
y_n<2>	in	LA_N_08	23
y_p<3>	in	LA_P_09	8
y_n<3>	in	LA_N_09	21
zclk_p	in	LA_P_17	3
zclk_n	in	LA_N_17	16
z_p<0>	in	LA_P_10	6
z_n<0>	in	LA_N_10	19
z_p<1>	in	LA_P_11	5
z_n<1>	in	LA_N_11	18
z_p<2>	in	LA_P_12	4
z_n<2>	in	LA_N_12	17
z_p<3>	in	LA_P_13	2
z_n<3>	in	LA_N_13	15

Table 6 : Camera Link Connector 2 (Base/Medium/Full Input Configuration)

6.1.3 Dual Base Output Configuration

Signal Name	Direction	FMC pin	SDR pin (Con. 1)
xclk_p	out	LA_N_18*	18
xclk_n	out	LA_P_18*	5
x_p<0>	out	LA_P_21	15
x_n<0>	out	LA_N_21	2
x_p<1>	out	LA_N_20*	16
x_n<1>	out	LA_P_20*	3
x_p<2>	out	LA_P_19	17
x_n<2>	out	LA_N_19	4
x_p<3>	out	LA_N_14*	19
x_n<3>	out	LA_P_14*	6
cc_p<1>	in	LA_N_00*	22
cc_n<1>	in	LA_P_00*	9
cc_p<2>	in	LA_P_04	10
cc_n<2>	in	LA_N_04	23
cc_p<3>	in	LA_N_03*	24
cc_n<3>	in	LA_P_03*	11
cc_p<4>	in	LA_P_02	12
cc_n<4>	in	LA_N_02	25
ser_tfg_p	out	LA_N_05*	21
ser_tfg_n	out	LA_P_05*	8
ser_tc_p	in	LA_N_15*	7
ser_tc_n	in	LA_P_15*	20

Table 7 : Camera Link Connector 1 (Dual Base Output Configuration)

Signal Name	Direction	FMC pin	SDR pin (Con. 2)
xclk_p	out	LA_N_11*	18
xclk_n	out	LA_P_11*	5
x_p<0>	out	LA_N_13*	15
x_n<0>	out	LA_P_13*	2
x_p<1>	out	LA_N_17*	16
x_n<1>	out	LA_P_17*	3
x_p<2>	out	LA_N_12*	17
x_n<2>	out	LA_P_12*	4
x_p<3>	out	LA_N_10*	19
x_n<3>	out	LA_P_10*	6
cc_p<1>	out	LA_N_01*	22
cc_n<1>	out	LA_P_01*	9
cc_p<2>	out	LA_P_08	10
cc_n<2>	out	LA_N_08	23
cc_p<3>	out	LA_N_07*	24
cc_n<3>	out	LA_P_07*	11
cc_p<4>	out	LA_N_06*	12
cc_n<4>	out	LA_P_06*	25
ser_tfg_p	in	LA_N_09*	21
ser_tfg_n	in	LA_P_09*	8
ser_tc_p	out	LA_N_16*	7
ser_tc_n	out	LA_P_16*	20

Table 8 : Camera Link Connector 2 (Dual Base Output Configuration)

6.1.4 Base/Medium/Full Output Configuration

Signal Name	Direction	FMC pin	SDR pin (Con. 1)
xclk_p	out	LA_N_18*	18
xclk_n	out	LA_P_18*	5
x_p<0>	out	LA_P_21	15
x_n<0>	out	LA_N_21	2
x_p<1>	out	LA_N_20*	16
x_n<1>	out	LA_P_20*	3
x_p<2>	out	LA_P_19	17
x_n<2>	out	LA_N_19	4
x_p<3>	out	LA_N_14*	19
x_n<3>	out	LA_P_14*	6
cc_p<1>	in	LA_N_00*	22
cc_n<1>	in	LA_P_00*	9
cc_p<2>	in	LA_P_04	10
cc_n<2>	in	LA_N_04	23
cc_p<3>	in	LA_N_03*	24
cc_n<3>	in	LA_P_03*	11
cc_p<4>	in	LA_P_02	12
cc_n<4>	in	LA_N_02	25
ser_tfg_p	out	LA_N_05*	21
ser_tfg_n	out	LA_P_05*	8
ser_tc_p	in	LA_N_15*	7
ser_tc_n	in	LA_P_15*	20

Table 9 : Camera Link Connector 1 (Base/Medium/Full Output Configuration)

Signal Name	Direction	FMC pin	SDR pin (Con. 2)
yclk_p	out	LA_N_11*	18
yclk_n	out	LA_P_11*	5
y_p<0>	out	LA_N_13*	15
y_n<0>	out	LA_P_13*	2
y_p<1>	out	LA_N_17*	16
y_n<1>	out	LA_P_17*	3
y_p<2>	out	LA_N_12*	17
y_n<2>	out	LA_P_12*	4
y_p<3>	out	LA_N_10*	19
y_n<3>	out	LA_P_10*	6
zclk_p	out	LA_N_07*	24
zclk_n	out	LA_P_07*	11
z_p<0>	out	LA_N_09*	21
z_n<0>	out	LA_P_09*	8
z_p<1>	out	LA_N_01*	22
z_n<1>	out	LA_P_01*	9
z_p<2>	out	LA_N_12*	23
z_n<2>	out	LA_P_12*	10
z_p<3>	out	LA_N_10*	25
z_n<3>	out	LA_P_10*	12

Table 10 : Camera Link Connector 2 (Base/Medium/Full Output Configuration)

6.2 Debug Pinout

Signal Name	Direction	FMC pin	Notes
led<0>	out	LA_P_25	Drive high to illuminate
led<1>	out	LA_P_26	Drive high to illuminate
led<2>	out	LA_P_27	Drive high to illuminate
led<3>	out	LA_P_28	Drive high to illuminate

Table 11 : LED Indicators

Signal Name	Direction	FMC pin	Notes
tx	out	LA_P_29	UART output
rx	in	LA_P_30	UART input
force	out	LA_P_32	Active high enable for RS232 interface
ready	in	LA_P_31	Active high
invalid_l	in	LA_P_33	Active low for framing error

Table 12 : RS232 Interface

Signal Name	Direction	J1 pin	Notes
txmon	out	1	RS232 compatible output
gnd		2	Ground
rxmon	in	3	RS232 compatible input

Table 13 : RS232 External

7 RS232 Electrical Specifications (J1)

The tables below show the electrical characteristics of the RS232 connection under typical operating conditions.

RX Inputs	Min	Tpy	Max	Units
Input Voltage Range	-25		25	V
Input Threshold Low	0.6	1.2		V
Input Threshold High	n/a	1.5	2.4	V
Input Hysteresis	n/a	0.5		V
Input Resistance	3	5	7	kΩ

Table 14 : RX input

TX Outputs	Min	Tpy	Max	Units
Output Voltage Swing	±5	n/a	±5.4	V
Output Resistance	300	n/a	10M	Ω
Output Short-Circuit Current	n/a	n/a	±60	mA
Output Leakage Current	n/a	n/a	±60	mA

Table 15 : TX output

Revision History

Date	Revision	Nature of Change
14th Sept. 2012	1.0	Initial Release
5th Aug. 2013	1.1	Correct SDR pins in Camera Link Connector 2 (Base/ Medium/Full Input Configuration)

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