



ALPHA DATA

ADA-VPX3-6T1
User Manual

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1 Introduction

The ADA-VPX3-6T1 is a high-performance OpenVPX FPGA processor card for applications using Virtex-6 FPGAs from Xilinx. This card supports all Virtex-6 LXT and SXT devices available in the FF(G)1759 package.

The card includes separate FPGA with a PCIe bridge developed by Alpha Data. Using a separate device allows high performance operation without the need to integrate proprietary cores in the user (target) FPGA.

The ADA-VPX3-6T1 is available in air-cooled and conduction-cooled configurations with optional 2 level maintenance configuration. View the ADA-VPX3-6T1 specification at [ADA-VPX3-6T1 Product Page](#) on www.alpha-data.com.

Basic Features

- 3U OpenVPX, compliant to VITA Standard 46.0 and 65
- Dedicated 4-lane Gen2 PCI-Express interface with 4 high-performance DMA controllers
- Virtex-6 FPGA in FF(G)1759 package
- 4 independent banks of DDR3-800 SDRAM, 256MB/bank, 1GB total (2GB option)
- Front-panel (XRM) interface with adjustable voltage, 146 free I/O signals and 8 MGT links to user FPGA
- VPX User I/O interface with 48 GPIO (36 can be driven differentially) signals and up to 16 Multi-Gigabit (MGT) links
- Two VPX control planes connected to target FPGA
- Two mSATA sites linked to target FPGA or VPX backplane
- Rear Transmission Module (RTM) breaks out all signals for accelerated development
- Voltage and temperature monitoring ([Health Monitoring](#))

Open VPX Compliance List

- SLT3-PAY-2F2U-14.2.3
- SLT3-PAY-1F1F2U-14.2.4
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-2F-14.2.7
- SLT3-PAY-1F4U-14.2.8
- SLT3-PAY-8U-14.2.9
- SLT3-PER-2F-14.3.1
- SLT3-PER-1F-14.3.2
- SLT3-PER-1U-14.3.3

1.1 References & Specifications

ANSI/VITA 42.0	XMC Standard, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.3	XMC PCI Express Protocol Layer Standard, June 2006, VITA, ISBN 1-885731-43-4
ANSI/VITA 46.0	VPX Baseline Standard, October 2007, VITA, ISBN 1-885731-44-2
ANSI/VITA 46.9	PMC/MXC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard, November 2010, VITA, ISBN 1-885731-63-9
ANSI/VITA 48.2	Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to VITA VPX, July 2010, VITA, ISBN 1-885731-60-4
ANSI/VITA 65	OpenVPX™ System Specification, June 2010, VITA, ISBN 1-885731-58-2
ANSI/IEEE 1386-2001	IEEE Standard for a Common Mezzanine Card (CMC) Family, October 2001, IEEE, ISBN 0-7381-2829-5
ANSI/IEEE 1386.1-2001	IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC), October 2001, IEEE, ISBN 0-7381-2831-7
ANSI/VITA 20-2001(R2005)	Conduction Cooled PMC, February 2005, VITA, ISBN 1-885731-26-4

Table 1 : References

2 Installation

2.1 Software Installation

Please refer to the Software Development Kit (SDK) installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

2.2 Hardware Installation

2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe SSD precautions:



- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2.2 System Requirements

The ADA-VPX3-6T1 is a 3U OpenVPX compliant FPGA card with FMC front IO interface. To use the Alpha Data's powerful API and drivers, the system controller must be capable of driving the PCIe lanes to the Bridge. The ADA-VPX3-6T1 also utilizes the OpenVPX 1000Base-X control lines, though this implementation is left to the user.

P2 complies with Vita 46.9 X24S+X8D+X12D user defined pin configuration with an additional 8 connections to P2 Row G. The X24s can be configured as either 24 single ended signals at 3.3V or 12 LVDS pairs. The eight

user defined single ended connections in row G are 3.3V compliant and can be isolated from the backplane via onboard switches.

Alpha Data offers a Rear Transition Module (RTM) that breaks out all P2 IO and P1 control lanes for use in lab and development environments (Part number: ADC-VPX3-XMC-RTM).

The ADC-VPX3-XMC can be configured to either utilize 5V or 12V as the main power source. The default build uses 12V, contact sales@alpha-data.com for details on the 5V build option.

2.2.3 Cooling Requirements

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the approximate current requirements for each power rail.

The board is supplied with a passive air cooled or conduction cooled heatsink according to the order number given at time of purchase. It is the users responsibility to ensure sufficient airflow for air cooled applications and appropriate chassis metalwork for conduction cooled applications.

The board features system monitoring that measures the board and FPGA temperature. It also includes a self-protection mechanism that will clear the target FPGA configuration if an over-temperature condition is detected.

See [Section 3.9](#) for health monitoring details.

3 Functional Description

3.1 Overview

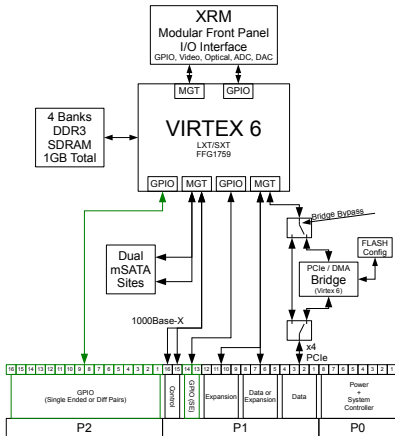


Figure 1 : ADA-VPX3-6T1 Block Diagram

Note:

The ADA-VPX3-6T1 is comprised of an ADM-XRC-6T1 XMC card mounted to an ADC-VPX3-XMC VPX carrier specifically designed to host Alpha Data XMCs. All reference to "XMC" refer to the ADM-XRC-6T1, while all references to "Carrier" refer to the ADC-VPX3-XMC.

3.2 Switch Definitions

There are three sets of eight DIP switches. One is placed on the XMC card and the other two are on the VPX Carrier. Their functions are described in tables below.

Note:

All switches are OFF by default with the exception of Carrier-SW1-2 which must be ON. All Factory Test and Reserved switches must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
XMC-SW1-1	Bridge Bypass	Bridge FPGA is bypassed - PCIe lanes (3:0) are connected directly to the user FPGA.	Bridge FPGA is used. PCIe lanes (3:0) are connected to the bridge.
XMC-SW1-2	Factory Test	Factory Test Mode	Normal Operation
XMC-SW1-3	E-Fuse	Enable E-Fuse programming voltage (VocEFuse = 2.5V)	Disable E-Fuse programming voltage (VocEFuse = 0V)
XMC-SW1-4	XMC JTAG	Connect JTAG chain to P5	Isolate JTAG chain from P5
XMC-SW1-5	Reserved	-	-
XMC-SW1-6	Flash Boot Inhibit	Target FPGA is not configured from onboard flash memory.	Target FPGA is configured from on-board flash memory.
XMC-SW1-7	Reserved	-	-
XMC-SW1-8	VPX Mode	Connect Tgt RearMGT(7:6) to P6	Connect Tgt RearMGT(7:6) to P5

Table 2 : XMC SW1 Definitions

3.3 LED Definitions

There are eight LEDs placed on the rear of the XMC board to indicate status:

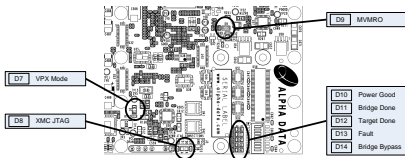


Figure 2 : XMC LED Locations

Comp. Ref.	Function	ON State	Off State
XMC-D7 (Amber)	VPX Mode	Tgt RearMGT(7:6) are connected to P6	Tgt RearMGT(7:6) are connected to P5
XMC-D8 (Amber)	XMC JTAG	On-board JTAG chain connected to P5	On-board JTAG chain is isolated from P5
XMC-D9 (Amber)	MVMRO	Inhibit writes to non-volatile memories	Enable writes to non-volatile memories.
XMC-D10 (Green)	Power Good	1.0V, 2.5V, 1.8V and 1.5V power supplies are on.	1.0V, 2.5V, 1.8V and 1.5V power supplies are not all on or all at their correct levels.
XMC-D11 (Green)	Bridge Done	Bridge FPGA is configured	Bridge FPGA is unconfigured
XMC-D12 (Green)	Target Done	Target FPGA is configured	Target FPGA is unconfigured
XMC-D14 (Amber)	Bridge Bypass	Bridge FPGA is bypassed - PCIe lanes (3:0) are connected directly to the user FPGA	Bridge FPGA is used. PCIe lanes (3:0) are connected to the bridge.
XMC-D13 (Red)	Fault	Voltage or Temperature Fault Detected.	No fault detected

Table 3 : XMC LED Definitions

3.4 VPX P0 Interface

3.4.1 MVMRO

Non-Volatile Memory Read Only. This signal is an input from the system. When asserted (high), all writes to non-volatile memories are inhibited. This is indicated by the Amber LED, XMC-D7.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the target FPGA.

3.4.2 SYSRESET#

XMC Reset In. This signal is an active low input from the system. When asserted, the bridge FPGA will be reset. This also acts as PCI Reset.

The SYSRESET# signal is translated to 1.8V levels and connected to the target FPGA at pin AF30.

3.4.3 AUXCLK

Auxiliary Clock. This clock is a direct input to the target FPGA. In OpenVPX this clock line is used for 1PPS synchronization signaling.

3.5 JTAG Interface

3.5.1 On-board Interface

A JTAG boundary scan chain is connected to header J3. This allows the connection of the Xilinx JTAG cable for FPGA debug using the Xilinx ChipScope tools.

The JTAG Header pinout is shown in Figure JTAG Header J2:

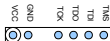


Figure 3 : JTAG Header J2

The scan chain is shown in Figure JTAG Boundary Scan Chain:

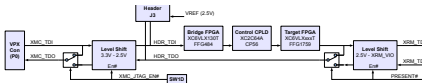


Figure 4 : JTAG Boundary Scan Chain

If the boundary scan chain is connected to the interface at the XMC connector (XMC-SW1-4 is ON), Header J3 should not be used.

3.5.2 VPX Interface

The JTAG interface on the VPX connector is normally unused with XMC_TDI and XMC_TDO floating.

The interface can be connected to the on-board interface (through level-translators) by switching XMC-SW1-4 ON. See table XMC SW1 Definitions

3.5.3 JTAG Voltages

The on-board JTAG scan chain uses 2.5V. The Vcc supply provided on XMC-J3 to the JTAG cable is +2.5V and is protected by a poly fuse rated at 350mA. 3.3V signals must not be used at header XMC-J3.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

The JTAG signals at the XRM2 interface use the adjustable voltage XRM_VIO.

3.6 Clocks

The ADA-VPX3-6T1 provides a wide variety of clocking options. The fixed reference clocks on the board can be combined with the PLLs in the FPGA to suit the target application.

The on-board clocks are detailed below.

Note:

Clock Termination

The LVDS clocks do not have termination resistors on the circuit board. On-die terminations in the FPGA must be enabled by setting the attribute "DIFF_TERM = TRUE". This can either be set in the source code when instantiating the buffer, or in the User Constraints File (UCF). See the Xilinx Virtex-6 Libraries Guide and Constraints Guide for further details.

3.6.1 REFCLK200M

The fixed 200MHz reference clock REFCLK200M is a differential clock signal using LVDS. It is connected to a Global Clock input on the Target FPGA at pins AE30 and AF30.

This clock can be used to generate application-specific clock frequencies using the PLLs within the Virtex-6 FPGA. It is also suitable as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK200M	IO_L0_GC_24	LVDS_25	AE30	AF30

Table 4 : REFCLK200M Connections

3.6.2 PCIe Reference Clock (PCIEREFCLK)

The 100MHz PCI Express reference clock is provided by the carrier card through the Primary XMC connector, P5 at pins A19 and B19. This is multiplied to 250MHz and distributed to both the Bridge and Target FPGAs. On the Target FPGA, it is connected to GTX Quad 113 and 114 to allow its use as a reference for all the MGT links to the XMC connectors. (See Figure MGT Clocks for details of the MGT reference clocks.)

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
PCIEREFCLK_1	MGTREFCLK1_113	LVDS_25	AD8	AD7
PCIEREFCLK_2	MGTREFCLK0_114	LVDS_25	AB8	AB7

Table 5 : PCIEREFCLK Connections

3.6.3 REFCLK250M

The fixed 250.0MHz reference, REFCLK250M, is a differential clock signal using LVDS. It is buffered and connected to three MGTREFCLK0 inputs on the Target FPGA at GTX Quad 113, 115 and 116. (See Figure MGT Clocks.)

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK250M_3	MGTREFCLK0_113	LVDS_25	AF8	AF7
REFCLK250M_2	MGTREFCLK0_115	LVDS_25	V8	V7
REFCLK250M_1	MGTREFCLK0_116	LVDS_25	M8	M7

Table 6 : REFCLK250M Connections

3.6.4 AUXCLK

Auxiliary Clock. This clock is a direct input to the target FPGA. In OpenVPX this clock line is used for 1PPS synchronization signaling.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
1PPS or AUXCLK	IO_L9_MRCC_33	LVDS	AK15	AK14

Table 7 : AUXCLK Connections

3.6.5 GCLK_M2C

The clock "GCLK_M2C" is a differential clock signal using LVDS. It is provided by an XRM module through the XRM connector, CN1, at pins 110 & 108. It is connected to a Global Clock input on the Target FPGA.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
GCLK_M2C	IO_L1_GC_24	LVDS_25	W30	V30

Table 8 : GCLK_M2C Connections

3.6.6 MGTCCLK_M2C

The reference clock "MGTCCLK_M2C" is a differential clock signal using LVDS. The clock is provided by an XRM module through the XRM connector, CN1, at pins 109 & 111. It is connected to GTX Quad 117 on the Target FPGA for application specific frequencies / line rates.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
MGTCCLK_M2C	MGTREFCLK0_117	LVDS_25	G10	G9

Table 9 : MGTCCLK_M2C Connections

3.6.7 XRM_PECL_CLK

The clock "XRM_PECL_CLK" is a differential clock signal using 2.5V PECL levels. The clock is provided by the target FPGA and connected to an XRM module through the XRM connector, CN1, at pins 113 & 115.

Signal	Target FPGA Output	IO Standard	"P" pin	"N" pin
XRM_PECL_CLK	IO_L11_MRCC_24	LPECL_25	R32	T32

Table 10 : XRM_PECL_CLK Connections

3.7 Flash Memory

A 512Mb Flash Memory (Intel / Numonyx PC28F512P30EF) is used to store board Vital Product Data (VPD), programmable clock parameters and configuration bitstreams for the Bridge and Target FPGAs.

The flash memory cannot be accessed by the target FPGA. Host access is only possible through the FLCTL, FLPAGE and FLDATA registers in the bridge FPGA.

Utilities for erasing, programming and verification of the flash memory are provided in the ADMXRC SDK.

Write Protect

The Flash Write Protect (WP#) pin is connected to an inverted version of the MVMRO signal at the XMC interface. When the MVMRO signal is active (High), all writes to the flash will be inhibited. This state will be indicated by the Amber LED, XMC-D9.

Alternate Bridge FPGA Bitstream		0x0000_0000
		0x007F_FFFE
		0x0080_0000
Default Bridge FPGA Bitstream		0x00FF_FFFE
		0x0100_0000
Vital Product Data (VPD)		0x0100_03FE
LCLK Word (15:0)		0x0100_0400
LCLK Word (31:16)		0x0100_0402
reserved		
B0 Length(7:0)	Boot Flag 0	0x0120_0000
Bitstream 0 Length(23:8)		0x0120_0002
reserved		
Default Target FPGA Bitstream (Target Bitstream 0)		0x0122_0000
		0x028F_FFFE
B1 Length(7:0)	Boot Flag 1	0x0290_0000
Bitstream 1 Length(23:8)		0x0290_0002
reserved		
Alternate Target FPGA Bitstream (Target Bitstream 1)		0x0292_0000
		0x03FF_FFFE

Figure 5 : Flash Memory Map

3.8 Configuration

3.8.1 Power-Up Sequence

If valid data is stored in the flash memory, the bridge will automatically set the programmable clock generator and configure the Target FPGA at power-up.

This sequence can be inhibited by turning the Flash Boot Inhibit (FBI) switch, XMC-SW1-6 to ON. (See Table XMC SW1 Definitions).

Note:

If an over-temperature alert is detected from the System Monitor, the target will be cleared by pulsing its PROG signal. See Section Automatic Temperature Monitoring.

3.9 Health Monitoring

The ADA-VPX3-6T1 has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using the Xilinx System Monitor (XSM) core within the Bridge FPGA and a National Semiconductor LM87 located on the board.

Control logic within the Bridge FPGA automatically scans the XSM and LM87 once per second and stores the current measurements in blockram.

The following voltage rails and temperatures are monitored:

Monitor	Purpose
1.0V	FPGA Core Supply (VccINT)
1.5V	DDR3 SDRAM, Target FPGA memory I/O
1.8V	Flash Memory, DC-DC converters for GTX Supplies
2.5V	FPGA Auxiliary Supply (VccAUX)
XRM_VIO	(Front-Panel) I/O voltage
3.3V	Board Input Supply
5.0V	Internally generated 5V supply
VPWR	Board Input Supply (either 5.0V or 12.0V)
Temp1	Target FPGA on-die temperature
Temp2	LM87 on-die temperature
Temp3	Bridge FPGA on-die temperature
Brg 1.0V	Bridge FPGA Core Supply (VccINT)
Brg 2.5V	Bridge FPGA Auxiliary Supply (VccAUX)

Table 11 : Voltage and Temperature Monitors

An example application that reads the system monitor ("sysmon") is available within the SDK.

3.9.1 Automatic Temperature Monitoring

At power-up, the control logic sets temperature limits and enables the over-temperature interrupt in the LM87. The temperature limits are shown in Table Temperature Limits:

	Target FPGA		Board (LM87)	
	Min	Max	Min	Max
Commercial	0 degC	+85 degC	0 degC	+70 degC
Extended	0 degC	+100 degC	0 degC	+85 degC
Industrial	-40 degC	+100 degC	-40 degC	+85 degC

Table 12 : Temperature Limits

Important:

If any temperature limit is exceeded, the Target FPGA is automatically cleared. This is indicated by Green LED D13 (Target DONE) switching off and Red LED, D14 (Fault) switching on.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

3.10 Local Bus

A Multiplexed Packet Transport Link (MPTL) connects the Bridge and Target FPGAs. It is capable of transferring data at up to 2GB/s simultaneously in each direction.

The MPTL replaces the parallel local bus used in previous generations of the ADM-XRC series. Details of the link and example designs are given in the Software Development Kit (SDK).

3.11 Target FPGA

3.11.1 I/O Bank Voltages

The Target FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in Table Target FPGA IO Banks. Full details of the IOSTANDARD required for each signal are given in the SDK.

IO Banks	Voltage	Purpose
0, 24	2.5V	Configuration, JTAG, LBus Control, XMC Control, Target SelectMap Interface
33, 34	2.5V	RGMII-100Base-X and VPX GPIO
37, 36, 26, 25	1.5V	DRAM Banks 0 & 1
27	1.5V	DRAM Banks 0 & 1, VPX GPIO
13, 12	1.5V	DRAM Bank 2, VPX GPIO
23, 32, 22	1.5V	DRAM Banks 2 & 3
14, 15, 16, 17	XRM_VIO	XRM2 Interface (variable voltage)

Table 13 : Target FPGA IO Banks (continued on next page)

IO Banks	Voltage	Purpose
21, 28, 38	1.5V	reserved

Table 13 : Target FPGA IO Banks

3.11.2 Target MGT Links

There are a total of 24 Multi-Gigabit Transceiver (MGT) links connected to the Target FPGA:

Links	Width	Connection
RearMGT(3:0)	4	Bridge FPGA (for MPTL) or VPX Connector P1 wafers (3:0) in Bridge Bypass Mode
RearMGT(5:4)	2	Direct link to VPX P1 wafers (5:4)
RearMGT(7:6)	2	Link to VPX P1, wafers (8:7) in default mode, connector P2 wafers (15:16) in VPX mode.
RearMGT(9:8)	2	Link to VPX P2, wafers (8:7) in remote ssd mode, FPGA connected to mSATA sites default mode.
RearMGT(15:10)	6	Direct link to VPX P2 lanes (7:0)
FrontMGT(7:0)	8	Direct link to XRM2 interface

Table 14 : Target MGT Links

The connections of these links are shown in Figure MGT Links:

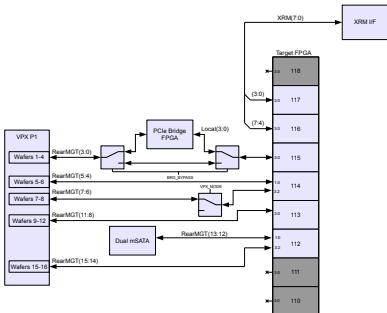


Figure 6 : MGT Links

Notes: (1)

The numbering in the Target FPGA refers to the GTX Quad number. Each Quad contains a grouping of four GTXE1 Multi-Gigabit Transceivers and two dedicated reference clock pairs.

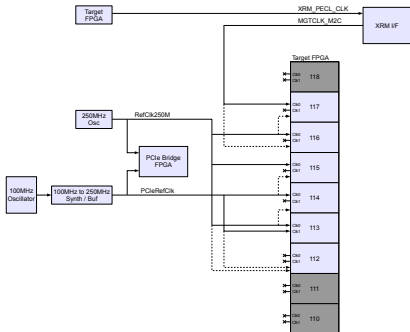


Figure 7 : MGT Clocks

3.12 Memory Interfaces

The ADA-VPX3-6T1 has four independent banks of DDR3 SDRAM. Each bank consists of two 16 bit wide memory devices in parallel to provide a 32 bit datapath capable of running up to 400MHz (DDR-800). 1Gb devices (Micron MT41J64M16-187E) are fitted as standard to provide 256MB per bank. 2Gb devices (giving 512MB per bank) are available as an ordering option.

The memory banks are arranged for compatibility with the Xilinx Memory Interface Generator (MIG). Figure DRAM Banks Shows the component references and FPGA banks used. Full details of the interface, signaling standards and an example design are provided in the SDK.

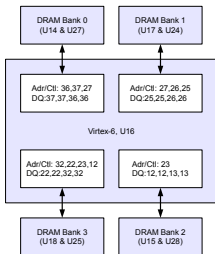


Figure 8 : DRAM Banks

3.13 XRM2 Interface and Front-Panel I/O

The XRM2 interface provides a high-performance and flexible front-panel interface through a range of interchangeable modules. Details of the XRM2 module range can be found on the Alpha Data website.

XRM2 modules are similar to the original XRM modules, but with connector CN1 rotated 180 degrees. (To prevent the accidental connection of older 3.3V modules.) In addition, all new XRM2 modules include an FRU PROM which provides information on the board type, serial number and voltage requirements. The bridge FPGA uses this information to automatically setup the correct VIO voltage level.

The XRM2 interface consists of two samtec connectors, CN1 and CN2.

3.13.1 XRM Connector, CN1

Connector CN1 is for general-purpose signals, power and module control. The connector is a 180-way Samtec connector with 3 fields.

The part fitted to the ADM-XRC-6T1 is Samtec QSH-090-01-F-D-A-K.

Full pinout information for this connector is listed in Appendix XRM Connector CN1, Field 1 to Appendix XRM Connector CN1, Field 3.

3.13.2 XRM Connector CN2

Connector CN2 is for the high-speed serial (MGT) links.

The part fitted to the ADM-XRC-6T1 is Samtec QSE-014-01-F-D-DP-A-K.

Full pinout information for this connector is listed in Appendix XRM Connector CN2.

3.13.3 XRM I/F - GPIO

The general purpose IO (GPIO) signals are connected in 4 groups to the Target FPGA. Each group consists of 16 standard I/O pairs, a Regional Clock Capable pair and either 2 or 4 single-ended signals. There are no on-board terminations on the pairs and any can be used in single-ended modes.

To allow fast data transfer, all of the GPIO signals within a group are delay matched to within 100ps.

All the XRM GPIO signals and FPGA IO banks share a common voltage, XRM_VIO, that can be either 2.5V, 1.8V or 1.5V. The required voltage is stored within the platform management PROM on the XRM.

Group	FPGA Bank	Name	Function
Group A	17	XRM_DA (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DA_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SA (1:0)	2 single-ended GPIO
Group B	16	XRM_DB (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DB_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SB (1:0)	2 single-ended GPIO
Group C	15	XRM_DC (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DC_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SC (1:0)	2 single-ended GPIO
Group D	14	XRM_DD (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DD_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SD (3:0)	4 single-ended GPIO

Table 15 : XRM GPIO Groups

3.13.4 XRM I/F - High-speed Serial Links

Eight MGT links are routed between the Target FPGA and the XRM2 interface. Lanes (6:0) are routed through the Samtec QSE-DP connector, CN2. Lane (7) is routed through the Samtec QSH connector, CN1.

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Appendix A: VPX Related Pin Assignments

Appendix A.1: Rear MGT Connections to the Target FPGA

In normal mode, the target FPGA RearMGT lanes (3:0) are connected to the Bridge FPGA. In Bridge Bypass Mode, they are connected to P5 lanes (3:0).

RearMGT Lanes (5:4) are connected directly to VPX wafers (5:4)

In normal mode, Lanes (7:6) are connector to P1 wafers (7:6). In VPX Mode, they are not connected.

RearMGT Lanes (11:8) are connected directly to VPX wafers (12:9)

RearMGT Lanes (13:12) are connected to the mSATA Sites.

RearMGT Lanes (15:14) are connected directly to VPX wafers (15:16)

See Figure MGT Links for clarity

The pin mappings are as follows in Table Target RearMGT Mapping

Signal	Tgt FPGA 'P' Pin	Tgt FPGA 'N' Pin
RearMGT_TX<0>	U1	U2
RearMGT_TX<1>	T3	T4
RearMGT_TX<2>	R1	R2
RearMGT_TX<3>	P3	P4
RearMGT_TX<4>	W1	W2
RearMGT_TX<5>	AA1	AA2
RearMGT_TX<6>	AC1	AC2
RearMGT_TX<7>	AE1	AE2
RearMGT_TX<8>	AG1	AG2
RearMGT_TX<9>	AH3	AH4
RearMGT_TX<10>	AJ1	AJ2
RearMGT_TX<11>	AK3	AK4
RearMGT_TX<12>	AL1	AL2
RearMGT_TX<13>	AM3	AM4
RearMGT_TX<14>	AN1	AN2
RearMGT_TX<15>	AP3	AP4
RearMGT_RX<0>	W5	W6
RearMGT_RX<1>	V3	V4
RearMGT_RX<2>	U5	U6
RearMGT_RX<3>	R5	R6

Table 16 : Target RearMGT Mapping (continued on next page)

Signal	Tgt FPGA 'P' Pin	Tgt FPGA 'N' Pin
RearMGT_RX<4>	Y3	Y4
RearMGT_RX<5>	AA5	AA6
RearMGT_RX<6>	AB3	AB4
RearMGT_RX<7>	AC5	AC6
RearMGT_RX<8>	AD3	AD4
RearMGT_RX<9>	AE5	AE6
RearMGT_RX<10>	AF3	AF4
RearMGT_RX<11>	AG5	AG6
RearMGT_RX<12>	AJ5	AJ6
RearMGT_RX<13>	AL5	AL6
RearMGT_RX<14>	AM7	AM8
RearMGT_RX<15>	AN5	AN6

Table 16 : Target RearMGT Mapping

Appendix A.2: GPIO

Signals beginning with GP can operate as single ended or differential. These signals pass through a FET bus switch. By limiting the signal voltage at 2.5V, these allow the use of 3.3V or 2.5V signalling levels to be used.

Signals beginning with SE are single ended and operate as 3.3V CMOS. These signals are level translated before reaching the FPGA.

Signal	VPX Connector. Pin	Target FPGA	Target FPGA	VPX Connector. Pin	Signal
GP1_P	P2.E1	BA16	BA17	P2.D1	GP1_N
GP2_P	P2.B1	AV16	AW16	P2.A1	GP2_N
GP3_P	P2.F2	AY15	AW15	P2.E2	GP3_N
GP4_P	P2.C2	AR14	AT14	P2.B2	GP4_N
GP5_P	P2.E3	AN14	AN13	P2.D3	GP5_N
GP6_P	P2.B3	AM13	AM12	P2.A3	GP6_N
GP7_P	P2.F4	AP11	AP12	P2.E4	GP7_N
GP8_P	P2.C4	AP13	AR13	P2.B4	GP8_N
GP9_P	P2.E5	AR12	AT12	P2.D5	GP9_N
GP10_P	P2.B5	AU12	AU13	P2.A5	GP10_N
GP11_P	P2.F6	AV13	AV14	P2.E6	GP11_N
GP12_P	P2.C6	AW12	AW13	P2.B6	GP12_N
GP13_P	P2.E7	BB13	BB14	P2.D7	GP13_N
GP14_P	P2.B7	BB16	BB17	P2.A7	GP14_N
GP15_P	P2.F8	BA15	BA14	P2.E8	GP15_N

Table 17 : VPX GPIO Signals (continued on next page)

Signal	VPX Connector. Pin	Target FPGA	Target FPGA	VPX Connector. Pin	Signal
GP16_P	P2.C8	AV15	AU14	P2.B8	GP16_N
GP17_P	P2.E9	AJ16	AJ15	P2.D9	GP17_N
GP18_P	P2.B9	AK18	AJ18	P2.A9	GP18_N
GP19_P	P2.F10	AM17	AM18	P2.E10	GP19_N
GP20_P	P2.C10	AJ17	AK17	P2.B10	GP20_N
GP21_P	P2.E11	AL17	AL16	P2.D11	GP21_N
GP22_P	P2.B11	AK15	AK14	P2.A11	GP22_N
GP23_P	P2.F12	AN18	AN19	P2.E12	GP23_N
GP24_P	P2.C12	AN16	AM16	P2.B12	GP24_N
GP25_P	P2.E13	AP18	AR19	P2.D13	GP25_N
GP26_P	P2.B13	AP16	AP17	P2.A13	GP26_N
GP27_P	P2.F14	AT17	AU18	P2.E14	GP27_N
GP28_P	P2.C14	AU19	AT19	P2.B14	GP28_N
GP29_P	P2.E15	AV18	AV19	P2.D15	GP29_N
GP30_P	P2.B15	AY18	AW18	P2.A15	GP30_N
GP31_P	P2.F16	BA19	AY19	P2.E16	GP31_N
GP32_P	P2.C16	BB18	BB19	P2.B16	GP32_N
GP1	P2.G1	BB38	BA36	P2.G3	GP2
GP3	P2.G5	AM34	AW41	P2.G7	GP4
GP5	P2.G9	AW36	AT40	P2.G11	GP6
GP7	P2.G13	AN36	AW42	P2.G15	GP8
GP9	P1.E14	AP35	AP38	P1.B14	GP10
GP11	P1.F14	AN38	BB39	P1.C14	GP12
GP13	P1.D13	BB36	BA42	P1.A13	GP14
GP15	P1.E13	AY42	AW41	P1.B13	GP16

Table 17 : VPX GPIO Signals

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Appendix B: Front (XRM) Connector Pinouts

The XRM interface consists of two connectors: CN1 and CN2. CN1 is a 180-way Samtec QSH in 3 fields. It is for general-purpose signals, power and module control. CN2 is a 28-way Samtec QSE-DP for high-speed serial (MGT) links.

Power
General Purpose I/O

Appendix B.1: XRM Connector CN1, Field 1

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DA_N0	N39	1	2	M39	DA_N1
DA_P0	N38	3	4	M38	DA_P1
DA_N2	T36	5	6	P40	DA_P3
DA_P2	U36	7	8	P41	DA_N3
DA_N4	L40	9	10	L42	DA_N5
DA_P4	L39	11	12	L41	DA_P5
DA_N6	T35	13	14	R42	DA_N7
DA_P6	T34	15	16	P42	DA_P7
DA_P8	R39	17	18	M41	DA_P9
DA_N8	P38	19	20	M42	DA_N9
DA_N10	P37	21	22	T40	DA_N11
DA_P10	N36	23	24	R40	DA_P11
DA_N12	R38	25	26	N40	DA_P13
DA_P12	T39	27	28	N41	DA_N13
DA_N14	M37	29	30	T41	DA_P15
DA_P14	M36	31	32	T42	DA_N15
DB_N0	Y37	33	34	V36	DB_N1
DB_P0	W37	35	36	W36	DB_P1
SA_0	N35	37	38	P36	
3V3	-	39	40	P35	
3V3	-	41	42	-	
3V3	-	43	44	-	2V5
5V0	-	45	46	-	VREF
5V0	-	47	48	-	VccIO
VBATT	-	49	50	-	VccIO
12V0	-	51	52	-	VccIO
12V0	-	53	54	-	M12V0
	-	55	56	-	
	-	57	58	-	
	-	59	60	-	

Table 18 : XRM Connector CN1, Field 1

Appendix B.2: XRM Connector CN1, Field 2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DB_N2	V39	61	62	U34	DB_N3
DB_P2	U39	63	64	V34	DB_P3
DB_N4	U38	65	66	V35	DB_N5
DB_P4	U37	67	68	W35	DB_P5
DB_N6	U33	69	70	W38	DB_N7
DB_P6	U32	71	72	V38	DB_P7
DB_N8	U41	73	74	V40	DB_P9
DB_P8	U42	75	76	W40	DB_N9
DB_P10	V33	77	78	W41	DB_N11
DB_N10	W33	79	80	V41	DB_P11
DB_N12	Y39	81	82	W42	DB_P13
DB_P12	Y40	83	84	Y42	DB_N13
DB_N14	Y35	85	86	AA39	DB_N15
DB_P14	AA35	87	88	Y38	DB_P15
	W32	89	90	AA34	SB_1
	Y33	91	92	AC38	SC_0
SA_1	R35	93	94	AD36	SC_1
SB_0	AA36	95	96	AG38	SD_0
	AD32	97	98	AB38	DC_N1
	AE32	99	100	AB37	DC_P1
DC_N0	AB36	101	102	AH34	
DC_P0	AC36	103	104	AJ35	
SD_1	AG36	105	106	AH35	SD_3
SD_2	AJ36	107	108	V30	
	G10	109	110	W30	
	G9	111	112	-	
	T32	113	114	-	
	R32	115	116	-	
	K3	117	118	J5	
	K4	119	120	J6	

Table 19 : XRM Connector CN1, Field 2

Appendix B.3: XRM Connector CN1, Field 3

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DC_P2	AC41	121	122	AA42	DC_P3
DC_N2	AD41	123	124	AB42	DC_N3
DC_N4	AC33	125	126	AB39	DC_P5
DC_P4	AC34	127	128	AA40	DC_N5
DC_P6	AD42	129	130	AC40	DC_P7
DC_N6	AE42	131	132	AD40	DC_N7
DC_N8	AD33	133	134	AB41	DC_N9
DC_P8	AE33	135	136	AA41	DC_P9
DC_P10	AF42	137	138	AD38	DC_N11
DC_N10	AF41	139	140	AE38	DC_P11
DC_P12	AB32	141	142	AD37	DC_N13
DC_N12	AB33	143	144	AE37	DC_P13
DC_N14	AE39	145	146	AL42	DD_P1
DC_P14	AE40	147	148	AM42	DD_N1
DD_P0	AK38	149	150	AE35	DC_N15
DD_N0	AJ38	151	152	AE34	DC_P15
DD_P2	AJ42	153	154	AM41	DD_N3
DD_N2	AK42	155	156	AL41	DD_P3
DD_N4	AG37	157	158	AG41	DD_N5
DD_P4	AF37	159	160	AF40	DD_P5
DD_P6	AK40	161	162	AL39	DD_N7
DD_N6	AL40	163	164	AK39	DD_P7
DD_N8	AF36	165	166	AH41	DD_N9
DD_P8	AF35	167	168	AG42	DD_P9
DD_N10	AJ40	169	170	AJ41	DD_N11
DD_P10	AH39	171	172	AH40	DD_P11
DD_N12	AF34	173	174	AG39	DD_N13
DD_P12	AG34	175	176	AF39	DD_P13
DD_N14	AG33	177	178	AK37	DD_N15
DD_P14	AF32	179	180	AJ37	DD_P15

Table 20 : XRM Connector CN1, Field 3

Appendix B.4: XRM Connector CN2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
	J1	1	2	H7	
	J2	3	4	H8	
	H3	5	6	G5	
	H4	7	8	G6	
	N1	9	10	P7	
	N2	11	12	P8	
	M3	13	14	N5	
	M4	15	16	N6	
	G1	17	18	F7	
	G2	19	20	F8	
	F3	21	22	E5	
	F4	23	24	E6	
	L1	25	26	L5	
	L2	27	28	L6	

Table 21 : XRM Connector CN2

Revision History

Date	Revision	Changed By	Nature of Change
12 Oct 2012	0.1	K. Roth	Initial Draft
6 Feb 2013	1.0	K. Roth	Initial Release
30 Jul 2014	2.0	K. Roth	Updated document to comply with latest ADC-VPX3-XMC carrier specification, XRM Appendix Corrected GCLK_M2C pins 108 and 110