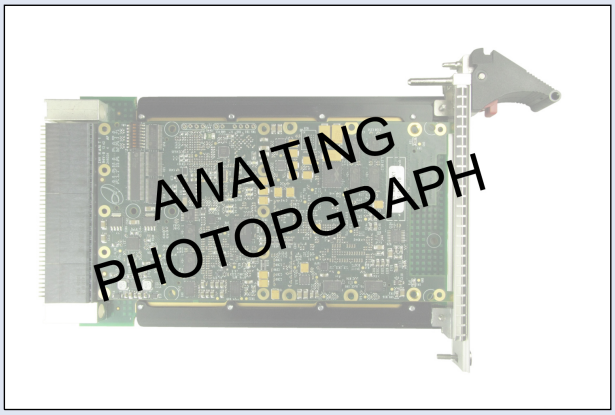
ADA-VPX3-6T1

ALPHA DATA

14th December 2010 **Datasheet Revision: 1.1**



Summary

The **ADA-VPX3-6T1** assembly brings together the power and configurability of the ADM-XRC-6T1 FPGA XMC in a VPX 3U module based on the Xilinx™ Virtex-6 range of Platform FPGAs.

Features include PCI Express® Gen2 interface, external memory, high density I/O, temperature monitoring, battery backed encryption and flash boot facilities.
A comprehensive cross platform API with support for **Microsoft Windows™**, **Linux** and **VxWorks** provides access to the full functionality of these hardware features.

Features

Applications:

Radar/Sonar Beamforming
ELINT
Image/Video Processing
Data Encryption

Target Devices:

Xilinx Virtex-6: LX240T, LX365T, LX550T, SX315T, SX475T (FFG1759)

Memory:

SDRAM - 1GByte in 4 independent banks (2GByte option) of DDR3 SDRAM @ 800MT/s (32-bit wide so 3.2GB/s)

FLASH - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.

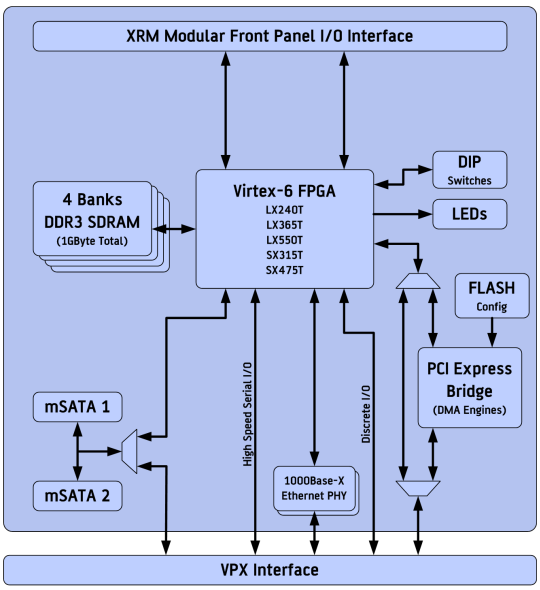
Front Connector I/O:

Up to 146 LVCMOS/LVDS I/O
Programmable signaling levels of 1.5V, 1.8V or 2.5V

8 High-Speed Serial Links

Rear Connector I/O:

P1 : 1 PCIe data plane. 2 expansion planes, 2 100BASE-BX control planes, 8 GPIO
P2 : 64 IO compliant with VITA 46.9 X64S



ADA-VPX3-6T1

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Specification	
Product Name	ADA-VPX3-6T1
Target Devices	Xilinx Virtex-6 - LX240T, LX365T, LX550T, SX315T, SX475T (FFG1759)
Host I/F	PCI Express® Gen2 x4
Interface	PCI Express® Gen2 x1, x2 or x4 link to separate bridge device with 2GB/s local link to user FPGA 4 DMA Controllers Interrupt Controller
Memory	**SDRAM** - 1GByte in 4 independent banks (2GByte option) of DDR3 SDRAM @ 800MT/s (32-bit wide so 3.2GB/s) **FLASH** - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.
Front I/O	Up to 146 LVCMOS/LVDS I/O Programmable signaling levels of 1.5V, 1.8V or 2.5V 8 High-Speed Serial Links
XRM2	The ADA-VPX3-6T1 is also available for XRM2 based FPGA products.
Rear I/O	**P1** : 1 PCIe data plane. 2 expansion planes, 2 100BASE-BX control planes, 8 GPIO **P2** : 64 IO compliant with VITA 46.9 X64S
Clocks	Low-jitter 250MHz reference clock, suitable for SerDes applications Low-jitter 200MHz reference clock for IOB delay circuits Custom clock inputs available through the XRM interface
Device Configuration	PCI Express® direct to SelectMAP port From Flash direct on power up External JTAG connector
Software	Drivers for Microsoft Windows™, Linux and VxWorks The ADM-XRC Gen3 SDK provides the example C and HDL source code, giving software engineers and FPGA designers a head start in creating applications.
Battery	Battery back-up for IP encryption keys
Environmental	**Temperature:** **Air cooled option (AC0)** Operating Temperature 0° to +55°C **Air cooled Extended Range (ACE)** Operating Temperature 0° to +55°C **Air cooled industrial option (AC1)** Operating Temperature -20° to +55°C **Conduction cooled option (CC1)** Operating Temperature -40° to 71°C **EMC:** FCC 47CFR Part 2 EN55022 Equipment Class B

Ordering Codes		
ADA-VPX3-6T1/z-y(m)(c)/Pn4		
Virtex-6 device	z	LX240T, LX365T, LX550T, SX315T, SX475T
Virtex-6 speed	y	1, 2, 3
Memory Size Fitted	m	blank = 256MBytes per bank - 1GBytes for the board, /2 = 512MBytes per bank - 2GBytes for the board, /4 = 1024MBytes per bank - 4GBytes for the board
Cooling	c	blank = air cooled commercial, /AC1 = air cooled industrial, /CC1 = conduction cooled industrial
Note	#	not all FPGA speed grades available in all configurations. Contact Alpha Data for full details.

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