ADC-VXS

VME/VXS DUAL PMC/XMC Carrier
VXS Xilinx Reconfigurable Computer

User Manual

Version 1.1

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1. Introduction

The ADC-VXS is a 6U VXS VMEbus compatible board that can carry two PCI Mezzanine Cards (PMCs), XMCs or hybrid PMC/XMC designs. The board can be configured as a simple PMC/XMC carrier card, or can be fitted with 2 Virtex5 FF1136 devices for bridging and/or processing capabilities. The board is highly versatile and supports many different possible configurations for processing data between the 7 main nodes.

- VME (Slave or Master)
- VXS (Payload)
- Gigabit front I/O (Optical or copper)
- PMC/XMC #1
- PMC/XMC #2
- On-board Virtex5 FPGA #1
- On-board Virtex5 FPGA #2

2. Standards

The ADC-VXS is designed to meet VITA 41.0-200x VXS VME Switched Serial Standard and ANSI/VITA1.1 VME64 Extensions.

The ADC-VXS card is designed for RoHS-6 compliance.

The ADC-VXS supports two PMC sites compliant to IEE1386-2001, ANSI/VITA35 Pn4 to P2 mapping, and ANSI/VITA 39-2003.

Additionally, each PMC/XMC site supports two XMC connectors compatible with VITA 42.0-2005 and VITA 42.2-2006 / VITA 42.3-2006.

Other relevant documents:

ANSI/VITA39 PCI-X for PMC/PrPMC

IEEE1101.2, and 1101.10 Mechanicals

Tundra Universe IID™ VME-to-PCI Bus Bridge User Manual

National Semiconductor LM87 Datasheet

3. Overview

The ADC-VXS Card is a 6U VXS carrier. It uses a Tundra Universe II bridge device to interface between a VME bus and a shared PCI bus capable of 33MHz operation. The PCI bus connects the two PMC sites, and one of the Virtex5 devices. The Universe bridge can also be isolated from the bus for PCI-X 100MHz operation.

The ADC-VXS Card has connections between the Jx4 connectors of each PMC site and the backplane P2 for conventional I/O or other VME P2 add on busses including RACE++. These connections are made in accordance to ANSI/VITA 35.

Two Virtex-5 devices can connect the PMC/XMC sites to the backplane fabric and provide the resources to support protocol conversion. There are also high speed switches to bypass the Virtex-5 devices for a direct connection to P0. Furthermore, these links are routed via high speed switches to allow 3 different configurations.

1. Each XMC site can simultaneously connect to the host (x4 lanes)
2. XMC #1 can connect to the host (x8 lanes)
3. XMC #1 can connect to to the host (x4 lanes) and XMC #1 can connect to XMC #2 (x4 lanes)

The ADC-VXS Card has Gigabit I/O on the front panel for optical (SFP) or copper (HSSDC2) connections. These serial links are routed via high speed switches to provide three different configurations.

1. Both Virtex-5 devices can interface with x2 full duplex lanes.
2. XMC site #2 can interface with x4 full duplex lanes.
3. Combination: XMC site #2 can interface with x2 full duplex lanes and one Virtex-5 can interface with x2 full duplex lanes.

In addition, the Jx6 connectors of each PMC/XMC site are cross-wired to allow direct high speed communication between XMC processor devices.

For debug purposes, the ADC-VXS has a JTAG interface that can be used to debug either or both PMC/XMC sites simultaneously with the ADC-VXS devices.

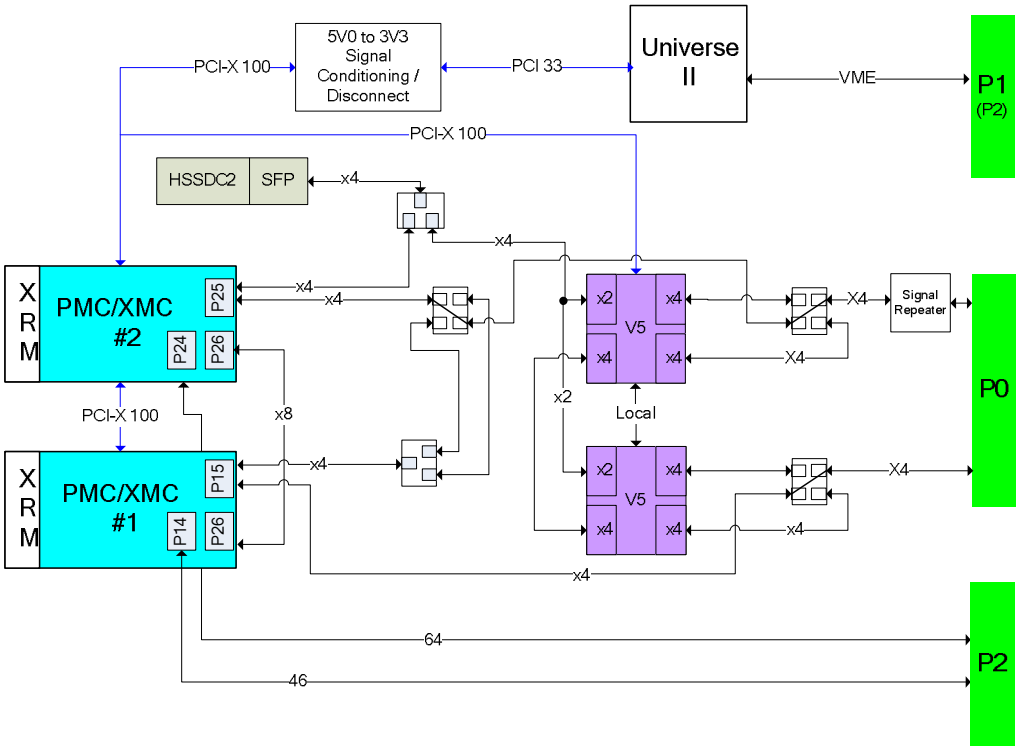

Figure 1 ADC-VXS Board Block Diagram

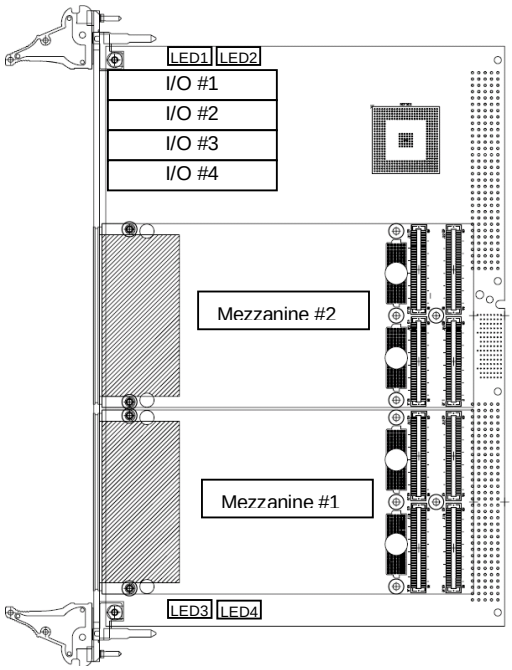

Figure 2 ADC-VXS Board Layout

Note. PMC #2 is the upper of the two PMC sites shown in the layout diagram above. PMC #1 is the lower in accordance with VITA35.

4. Hardware Installation

This chapter explains how to install the ADC-XVS into a VXS system motherboard.

4.1. Host System requirements

The ADC-VXS is compatible with VME systems and VXS payload slots. The ADC-VXS must be installed in a motherboard that supplies +5.0V power to the VME connectors. +12V and -12V may also be required for certain PMC/XMC modules. If the host system provides +3.3V power, then ensure that jumper JP3 is not fitted. If the host system doesn't provide a +3.3V power supply and no other boards installed in the system will pull power from this rail, then fit JP3 to enable the on board power supply.

4.2. Handling instructions

Observe ESD precautions when handling the cards to prevent damage to components by electrostatic discharge.

Avoid flexing the board.

4.3. Board Jumper Settings

The ADC-VXS board contains 4 jumpers and 4 switches to set various modes and configurations. Any adjustments to these settings should be made prior to installation.

Default Setting ⊙

SWITCH	**FUNCTION**	**RANGE**	**VME ADDR**
SW1	Lower VME Address (Register Access Image – See Universe II Manual)	Hex 0x0 : 0xF	VA[24:21] (Lower 4 bits according to address mode)
SW2	Upper VME Address (Register Access Image – See Universe II Manual)	Hex 0x0 : 0xF	VA[28:25] (Upper 4 bits according to address mode)
JUMPER	**FUNCTION**	**Jumper Fitted (ON)**	**Jumper Removed (Off)**
JP1	Master Reset	Reset	Normal ⊙
JP2	Universe bridge PCI enable	Disconnect PCI bus	Connect Universe ⊙
JP3	3.3V On Board Power Supply Enable	Enable	Disable ⊙
JP4	CPLD Program	Enable (for factory use)	Normal (Forward JTAG Debug Chain) ⊙
SWITCH	**FUNCTION**	**Switch ON (Closed)**	**Switch OFF (Open)**
SW3-1	VME64 Auto ID Mode	Enabled	Disabled ⊙
SW3-2	DY4 Auto ID Mode	Enabled	Disabled ⊙
SW4-1	XMC 2 Non-Volatile Memory Write Protect	Not-Protected ⊙	Protected
SW4-2	XMC 1 Non-Volatile Memory Write Protect	Not-Protected ⊙	Protected
SW4-3	XMC BRG2 Mux Select	Route Lanes to FPGA	Bypass ⊙
SW4-4	XMC BRG1 Mux Select	Route Lanes to FPGA	Bypass ⊙
SW4-5	XMC P25 Mux Select	Route Lanes from P15 Mux	Route P25 to BRG2 Mux ⊙

SWITCH	FUNCTION	Switch ON (Closed)	Switch OFF (Open)
SW4-6	XMC P15 Mux Select	Route Lanes to P25*	Route P15 to BRG1 Mux* ⚙
SW4-7	XMC FPIO 0-1 Mux Select	Route Lanes to Virtex5 2	Route to P25 ⚙
SW4-8	XMC FPIO 2-3 Mux Select	Route Lanes to Virtex5 1	Route to P25 ⚙
SW5-1	JTAG Select (ADC-VXS Devices)	Bypass	Include in Chain ⚙
SW5-2	JTAG Select (PMC2 Header)	Bypass	Include in Chain (If present) ⚙
SW5-3	JTAG Select (PMC1 Header)	Bypass	Include in Chain (If present) ⚙
SW5-4	REFCLK Frequency Select	125MHz	100MHz ⚙
SW5-5	Monarch Function Enable PMC 2 **	Enable	Disable ⚙
SW5-6	Monarch Function Enable PMC 1 **	Enable	Disable ⚙
SW5-7	XMC2 Root Complex***	Enable	Disable ⚙
SW5-8	XMC1 Root Complex***	Enable	Disable ⚙
SW6-1	25MHz Configuration Clock Enable	Always Enabled	Auto Enabled ⚙
SW6-2	Virtex5 #2 Configuration Mode	From Flash SelectMap⚙	From Virtex5 #1 Serial
SW6-3	Virtex5 #1 Configuration Mode	From Flash SelectMap⚙	From Virtex5 #2 Serial
SW6-4	Unused	N/A	N/A

* When SW4-5 is ON these lanes are routed, else disconnected
** Monarch signal is used to enable processor PMC master features (bus enumeration).
*** Root signal is used to enable a processor XMC root features (bus enumeration). It also enables the carrier card to propagate the XMC (Reset) MRSTOn to both XMC sites MRSTIn.

SWITCH	FUNCTION	00*	01*	10*	11*
SW3-4 / SW3-3	VME Address Mode	A16 ⚙	A24	A32	Reserved

* Note: {1= Switch ON (Closed) 0 = Switch OFF (Open)}

Table 1 Switch and Jumper Quick Reference

4.4. Installing the ADC-VXS into a VME/VXS system

Note: This operation should not be performed while the motherboard is powered up.

The PMC/XMC modules must be secured to the ADC-VXS using M2.5 screws in the four holes provided. The ADC-VXS uses a key pin to prevent 5V PMC signalling devices from being installed, and care should be taken to comply with the 3.3V signalling level. The PMC bezel through which the I/O connector protrudes should be flush with the front panel of the ADC-VXS.

5. Software Installation

Please refer to the SDK installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

6. Board Description

6.1. VME Interface

The ADC-VXS connects to the VME bus using the Tundra Universe IID bridge

bridge and a set of 74ABT family bus transceivers. The ADMXRC_SDK driver configures the images and registers of the Universe IID bridge for slave mode. The driver will configure the bridge for API support in VxWorks.

6.1.1. Reset

The ADC-VXS is normally reset by the VMEBUS through the Tundra Universe IID bridge. The board also has a 2 pin jumper that can connect to a push button for user reset to the bridge master reset input.

The on board CPLD asserts the PCI/PCI-X bus reset when any reset is detected from the Universe II bridge, or from the PMC sites.

6.1.2. Configuration

The ADC-VXS can support both VME slave and VME master operation. See the Universe IID user manual for information on setting the necessary images and registers for master mode.

The VME Slave supports A16, A24, and A32 address spaces and D8, D16, D32, and D64 data transfer sizes. Note: for 64-bit data transfers, the address bus[31:1], VLWORD signal, and data bus[31:0] are used to from the 64-bit data path.

As a VME Master the ADC-VXS can generate A16, A24, and A32 VMEbus address cycles and D8 even, D8 odd, D16, D32, and D64 data transfers.

The VME base address is selected via 2 rotary encoding switches, which sets the top 8 bits of the address in A32 and A24 modes, and the top 5 bits in A16 mode. The addressing mode is selected via 4 DIP switches.

6.1.3. VME Serial Interface Support

The serial utility bus signals from the VME connectors are connected to both Virtex5 FPGA devices. The connection includes signal conditioning for 5V levels on the serial busses. The 6 supported serial signals are: SERA and SERB signals from VME P1, and PA_SCL, PA_SDA, PB_SBL, PB_SDA from VME P0.

6.1.4. Keying

The ADC-VXS Card complies with the keying requirements for VXS cards and supports both A0 and K0.

A0 by default has the value “1”.

K0 is colour steel blue (key 1256) for VXS.4 PCI Express.

K0 is colour pale orange (key 1247) for VXS.2 Serial RapidIO.

6.2. PMC/XMC Sites

The ADC-VXS Card provides two PMC/XMC sites. These sites have the full set of PMC and XMC connectors and are named [J11,J12,J13,J14,J15,J16] and [J21,J22,J23,J24,J25,J26] for site 1 and site 2 respectively. These are subsequently referred to as Jx1, Jx2, Jx3, Jx4, Jx5 and Jx6 when used for either site.

6.2.1. PCI Central Resources

6.2.1.1 Arbiter

The ADC-VXS Card contains a PCI arbiter capable of allocating the bus to 6 devices in a round-robin priority scheme. This configuration supports PrPMC cards which contain 2 REQ/GNT lines each.

6.2.1.2 PCI Clock

The ADC-VXS Card is fitted with a fixed 33MHz oscillator which is buffered and routed to all PCI devices. There is also a clock synthesiser which can source 66MHz and 100MHz as different PCI modes are detected by the central resource.

6.2.1.3 PCI Mode Support

The central resource CPLD device is capable of auto-detecting the type of protocol supported by the plugged-in PMCs. The board has circuitry to detect levels of PCIXCAP and M66EN to determine the type and speed of bus. The central resource will automatically set the correct clock frequency and provides the PCI-X initialization pattern to the bus.

In addition, 32 or 64 bit PCI bus widths are supported and these too are auto-detected using standard procedures.

Only PCI at 33MHz is available in the VME configuration when using the Universe IID bridge. This limitation is also auto-detected by the central resource.

6.2.2. PrPMC Support

The ADC-VXS is capable of supporting a PrPMC as the bus controller. There are 2 DIP switches to assert the Monarch signals to the Jx2 connectors.

6.2.3. PCI Bus Interrupt / IDSEL Mapping

The PCI bus interrupts are mapped starting with PMC site #2 as the typical master. The following table describes the interconnects between the system interrupts and the different devices, along with the IDSEL connection to the address bus.

Device	IDSEL	1	2	3	4
PMC #2	AD16	A	B	C	D
PMC #1	AD17	D	A	B	C
UniverseIID	AD18 - Optional fit for PCI Slave	A*	B*	C*	D*
Virtex5	AD19	B*	C*	D*	A*
PMC #2 B	AD20	A	B	C	D
PMC #1 B	AD21	D	A	B	C

* User Programmable

Table 2 PCI Interrupt Map

6.2.4. Jx4 Interfaces

The ADC-VXS is compatible with FPGA cards that provide signalling on Jx4 and provides a path that connects J14 and J24 to VME connector P2 using a direct route without any other circuits in place. The signals are wired in accordance with VITA35.

PMC #1 is configured using VITA35 P4V2-46dz.

PMC #2 is configured using VITA35 P4V2-64ac.

6.2.5. Jx5 Primary XMC Interface

The ADC-VXS Card routes 4 pairs of TX and RX serial signals from each XMC site, through an LX110T, and to the high speed P0 connector as shown in Figure 1. These links can also bypass the LX110T devices for a direct connection to P0.

MGT resources in the LX110T's are allocated to support use of the embedded PCIe hard core on the P0 interfaces

A clock source is provided on the ADC-VXS using a 125MHz reference oscillator and this is fed through a PLL to provide buffered reference clocks to the REFCLK inputs on each of the Jx5 connectors and also the GTP refclk inputs to the respective LX110T devices. The frequency output by the PLL is selected by a CPLD on the ADC-VXS and, by default, 100MHz is produced. This can be changed via a DIP switch to 125MHz and other frequencies are available with a CPLD firmware change. See section 6.3.4 for further details on the programmable clock.

6.2.6. XMC Jumper Options

The ROOT signal can be asserted on either J15 or J25 by DIP switches for PrXMC support. The CPLD on the ADC-VXS will detect these signals and alter the reset strategy of the XMC sites to accept the MRSTO signal and assert the MRSTI signals on the Jx5 connections.

The NVMRO signals can be asserted on either J15 or J25 by DIP switches to prevent memory writes on the XMC boards.

6.2.7. Jx6 Secondary XMC Interface

The J16 and J26 connectors are configured to allow high speed communication between XMC sites local to the carrier card.

There are 8 channels of TX/RX provided between the two secondary XMC connectors, sufficient for x8 PCI Express or other serial protocols. A reference clock is provided to Jx5, for XMC signalling.

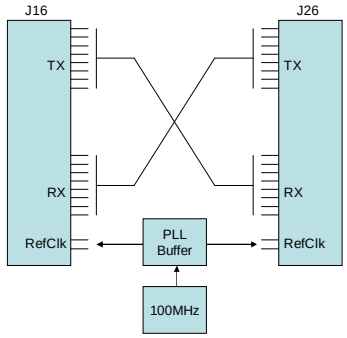

Figure 3 J16/J26 Interconnect

6.2.8. Power Resources

Power is supplied to the PMC and XMC connectors directly from the VME backplane connectors for the +5V, +12V and -12V rails. 3.3V power is also supplied from the VME backplane connectors if available, or via an on-board power supply of the ADC-VXS. There is a jumper that must be installed to enable this power supply, and it should only be used if the VME bus does not provide this supply and no other loads are connected to the 3.3V power pins of the VME system.

6.3. Virtex-5 Resources

6.3.1. Local Bus

There is a 64 bit local bus connecting the 2 Virtex-5 devices, with either capable of being the master. This multi-master local bus between the bridge and the target FPGA can use a 32-bit or 64-bit multiplexed address and data path. There are also x4 full duplex Gigabit links between the 2 FPGAs for a high speed local bus.

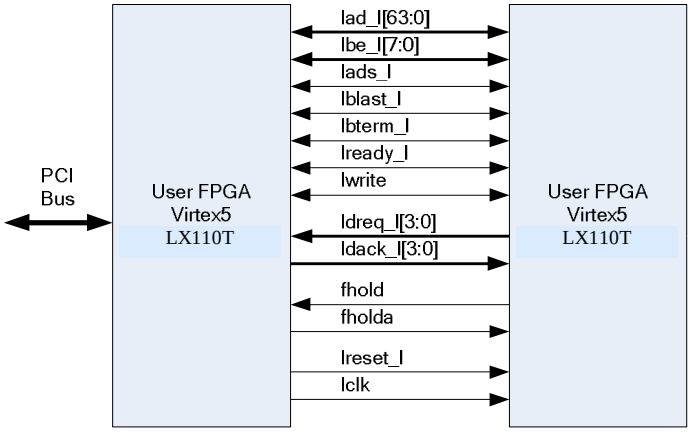

Figure 4 Local Bus Interface

Signal	Type	Purpose
lad[63:0]	bidir	Address and data bus.
lbe_l[7:0]	bidir	Byte qualifiers
lads_l	bidir	Indicates address phase
lblast_l	bidir	Indicates last word
lbterm_l	bidir	Indicates ready and requests new address phase
lready_l	bidir	Indicates that target accepts or presents new data
lwrite	bidir	Indicates a write transfer from master
ldreq_l[3:0]	unidir	DMA request from target to bridge
ldack_l[3:0]	unidir	DMA acknowledge from bridge to target
fhold	unidir	Target bus request
fholda	unidir	Bridge bus acknowledge
lreset_l	unidir	Reset to target
lclk	unidir	Clock to synchronise bridge and target

Table 3 Local Bus Interface Signal List

6.3.2. DDR2 DRAM

Each Virtex-5 Device supports 2 banks of DDR2 SDRAM x 32 bits. Each bank consists of two memory devices in parallel to provide a 32 bit datapath. 1Gb Micron MT47H64M16 devices are fitted as standard to provide 256MB per bank (1GB total for the board). The board will support higher capacity memory devices, for upgrades at order time. The ADC-VXS has been designed for compatibility with Xilinx memory interface cores.

Details of the DDR2 signalling standards are given in the table below:

Name	Direction	I/O Standard
DDR_ad[15:0], DDR_ba[2:0], DDR_rasn, DDR_casn, DDR_wen, DDR_csn, DDR_cke, DDR_odt	Output	SSTL18_I_DCI
DDR_ck0,	Output	DIFF_SSTL18_II

DDR_ckn0		
DDR_dq[31:0]	BiDir	SSTL18_II
DDR_dm[3:0]	Output	SSTL18_I
DDR_dqs[3:0], DDR_dqsn[3:0]	BiDir	DIFF_SSTL18_II
DDR_ck1, DDR_ckn1	Output	DIFF_SSTL18_II

Table 4 DDR2 Memory Bank Configuration

6.3.3. Programming

Each Virtex-5 Device has a 32Mb XC32F platform flash for device programming, and a 32Mb SPI flash. Both FPGAs can be configured from their corresponding platform flash via SelectMAP, or one FPGA can program the other via the serial interface. There is a dedicated 25MHz oscillator for the programming interface which drives all of these devices. The oscillator will auto-disable after both FPGAs are configured. It can also be used as a user clock by closing SW6-1 to keep it enabled. The ADC-VXS Board has 2 DIP switches SW6-2, SW6-3 to select the programming modes of the FPGAs. E.g. closing the corresponding switch will configure the FPGA from its flash device.

6.3.4. Clocks

The ADC-VXS Board provides a 200MHz reference oscillator for IODELAY calibration and user clocks. The board also provides a GTP reference clock with 8 selectable frequencies. There is dedicated routing between the 2 FPGAs for LCLK signalling. Either device can act as the local bus bridge, and generate the LCLK to the other.

The GTP clock synthesiser has 2 banks of clock outputs, each with a selectable frequency. Each bank is routed to one Virtex5 FPGA and the adjacent XMC site (Jx5 connector reference clock, GTP dedicated clock X0Y5, and GTP dedicated clock X0Y2). The clock signals to the GTP inputs are terminated and AC coupled in accordance with Xilinx guidelines. The clocks to the XMC connectors are AC coupled and terminated in accordance with PCI-Express specifications. The frequency select signals for each bank are routed to the CPLD, and can be customized by a firmware change from the factory.

N[2:0]	DIV	f	Default Selection
000	1	500MHz	
001	2	250MHz	
010	3	167MHz	
011	4	125MHz	SW5-4 ON
100	5	100MHz	SW5-4 OFF
101	6	83MHz	
110	8	62.5MHz	
111	10	50MHz	

Table 5 Programmable Clock Outputs

6.3.5. Health Monitoring

The ADC-VXS has the ability to monitor temperature and voltage of key parts of the board to maintain a check on the operation of the board. The monitoring is implemented by a National Semiconductor LM87 and is supported by the board control logic connected using I^2C accessible from either Virtex-5

The following supplies and temperatures, as shown in Table 6, are monitored.

Monitor	LM87 Register	Purpose
1.0V	0x21	User FPGA Core Supply
1.8V	0x29	Memories, User FPGA Memory I/O, Local Bus I/O, PCIe signal repeater
2.5V	0x28	Source voltage for FPGA VCCAUX
3.3V	0x22	Board Input Supply / On board supply
5.0V	0x23	Board Input Supply
12.0V	0x24	Board Input Supply
Temp1	0x26	User FPGA die temperature
Temp2	0x20	User FPGA die temperature
Temp3	0x27	LM87 on die temperature for board/ambient

Table 6 Voltage and Temperature Monitors

6.3.6. SFP Control / Status Signals

Each of the 4 SFP modules has a set of control / status signals connected to the corresponding Virtex5 device (Upper FPGA - U19 to I/O 1 & I/O 2 | Lower FPGA – U36 to I/0 3 & I/0 4) shown in Figure 2. These signals are all optional and all have pull-up or pull-down resistors to set the default values.

Signal	Direction (relative to FPGA)	Default (Pull-up / Pull-down)	Description
TX_Fault	Input	PU	Transmitter Fault Indication
TX_Disable	Output	PD	Transmitter Disable
SFP_Present_n	Input	PU	Indicates that the module is present
LOS	Input	PU	Loss of Signal
Rate_Select	Output	PU	Receiver bandwidth select (H = full, L=reduced)
MSD	Output	PU	Serial Data
MSCL	Output	PU	Serial Clock

Table 7 SFP Control / Status Signals

6.3.7. LED Indicators

Each Virtex5 FPGA controls 2 dual colored (Red / Green) LED indicators. These signals are active low, and are connected directly to the FPGA. They can be used for activity / fault indicators for the front panel I/O, or for other user functionality. The dual colored LEDs can be driven simultaneously to produce orange or different mixes using a PWM type signal. LED1 and LED2 are driven by the upper FPGA (U19) and LED3 and LED4 are driven by the lower FPGA (U36), shown in Figure 2.

6.3.8. PCIe Repeater Control Signals

Each of the channels on the P0 primary interface is routed through a PI2EQX4402 PCIe signal repeater as shown in Figure 1. This provides the necessary signal integrity for applications using 2 or more multiplexors on the ADC-VXS board. Channels 1-4 control the Rx signals from the VXS host, and channels 5-8 control the Tx signals to the VXS host. The ADC-VXS board has resistor pull-downs to select the default settings. The control signals are also routed to the upper FPGA (U19)

Output Swing Control

SEL3_[A:D]	SEL4_[A:D]	Swing
0	0	1x (default)
0	1	0.8x
1	0	1.2x
1	1	1.4x

Output De-emphasis Adjustment

SEL5_[A:D]	SEL6_[A:D]	De-emphasis
0	0	0dB
0	1	-2.5dB
1	0	-3.5dB (default)
1	1	-4.5dB

Equalizer Selection

SEL0_[A:D]	SEL1_[A:D]	SEL2_[A:D]	Compliance Channel
0	0	0	No Equalization
0	0	1	[0:1.5dB] @ 1.25 GHz
0	1	0	[0:2.5dB] @ 1.25 GHz
0	1	1	[0:3.5dB] @ 1.25 GHz (default)
1	0	0	[0:4.5dB] @ 1.25 GHz
1	0	1	[0:5.5dB] @ 1.25 GHz
1	1	0	[0:6.5dB] @ 1.25 GHz
1	1	1	[0:7.5dB] @ 1.25 GHz

Table 8 Signal Repeater Settings

6.3.9. I/O Bank Voltages

Bank	Voltage	Description
0	3.3V	Configuration I/F
3	2.5V	Reference Clocks
4	3.3V	Local Clocks
2, 6, 25	3.0V	PCI Interface, SelectMAP I/F (FPGA #1 only)
2	3.3V	SelectMAP I/F (FPGA #2 only)
19	3.3V	Health Monitor, VME serial management bus, FPIO control, LED control

5, 11, 15, 23	1.8V	DDR2 SDRAM
22	3.3V	Programming, Serial Flash
13,17,21	1.8V	Local Bus
12, 20	1.8V	Mux Control, PCIe Repeater Control
1, 18	1.8V	Unused

Table 9 User FPGA I/O Bank Voltages

6.4. Copper / Optical Front Panel I/O Interfaces

4 Copper or Optical interfaces are provided via the front panel using SFP modules or HSSDC2 connectors. Each Virtex5 FPGA provides an interface to two channels. The links can also be routed to XMC site #1 connector J15, and bypass the Virtex5 FPGAs.

The Virtex-5 Devices are able to interface with the SFP control signals, and drive 4 LED's each.

6.5. JTAG Debug

The ADC-VXS features a versatile JTAG debugging chain that has selectable routing to the carrier card devices, and either of the PMC JTAG headers. The main JTAG connector (J1) connects to a Xilinx Parallel IV or Xilinx Platform Cable USB using the IDC ribbon cable provided with these devices.

There are 2 JTAG headers (J11 and J12) which allow connections to the PMC/XMC cards' JTAG chains by using flying leads which are available from Xilinx. The I/O voltage of the JTAG header signals is controlled by the VCC signal from the PMC, and is supported from 2.5V to 5.0V.

There are 3 switches on the ADC-VXS that control the routing of the JTAG chain. When the corresponding switch is closed, the devices will automatically be inserted into the JTAG chain in the following order: SW5-1 will include the both Virtex5 devices, both platform flash devices and the Universe IID bridge in the chain, SW5-2 will include the PMC1 header in the chain, and SW5-3 will include the PMC2 header in the chain. When the corresponding switch is open, the JTAG signals will be set in an idle state and the JTAG chain routed around them.

The PMC JTAG headers have an auto-detect feature that will remove them from the JTAG chain if the header is not connected.

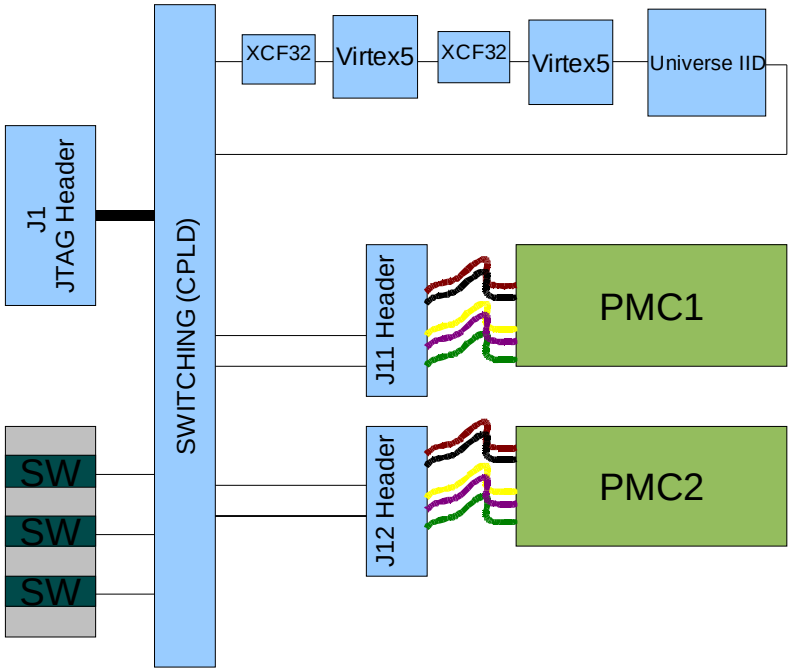

Figure 5 JTAG Routing

7. Connector Pin Assignments

7.1. VME P0

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	PA_SCL	GND	DP2-	DP2+	GND	DP1-	DP1+
2	GND	DP4-	DP4+	GND	DP3-	DP3+	GND
3	PA_SDA	GND	DP6-	DP6+	GND	DP5-	DP5+
4	GND	DP8-	DP8+	GND	DP7-	DP7+	GND
5	NC	GND	NC	NC	GND	NC	NC
6	GND	NC	NC	GND	NC	NC	GND
7	NC	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND
9	NC	GND	NC	NC	GND	NC	NC
10	GND	NC	NC	GND	NC	NC	GND
11	PEN_L	GND	NC	NC	GND	NC	NC
12	GND	DP24-	DP24+	GND	DP23-	DP23+	GND
13	PB_SCL	GND	DP26-	DP26+	GND	DP25-	DP25+
14	GND	DP28-	DP28+	GND	DP27-	DP27+	GND
15	PB_SDA	GND	DP30-	DP30+	GND	DP29-	DP29+

Table 10 VME P0 Pinout

7.2. VME P1

Pin	Row z	Row a	Row b	Row c	Row d
1	NC	D00	BBSY*	D08	+5V
2	GND	D01	BCLR*	D09	GND
3	NC	D02	ACFAIL*	D10	NC
4	GND	D03	BG0IN*	D11	NC
5	NC	D04	BG0OUT*	D12	NC
6	GND	D05	BG1IN*	D13	NC
7	NC	D06	BG1OUT*	D14	NC
8	GND	D07	BG2IN*	D15	NC
9	NC	GND	BG2OUT*	GND	NC
10	GND	SYSCLK	BG3IN*	SYSFAIL*	NC
11	NC	GND	BG3OUT*	BERR*	NC
12	GND	DS1*	BR0*	SYSRESET*	+3.3V
13	NC	DS0*	BR1*	LWORD*	NC
14	GND	WRITE*	BR2*	AM5	+3.3V
15	NC	GND	BR3*	A23	NC
16	GND	DTACK*	AM0	A22	+3.3V
17	NC	GND	AM1	A21	NC
18	GND	AS*	AM2	A20	+3.3V
19	NC	GND	AM3	A19	NC
20	GND	IACK*	GND	A18	+3.3V
21	NC	IACKIN*	SERA	A17	NC
22	GND	IACKOUT*	SERB	A16	+3.3V
23	NC	AM4	GND	A15	NC
24	GND	A07	IRQ7*	A14	+3.3V
25	NC	A06	IRQ6*	A13	NC
26	GND	A05	IRQ5*	A12	+3.3V

27	NC	A04	IRQ4*	A11	NC
28	GND	A03	IRQ3*	A10	+3.3V
29	NC	A02	IRQ2*	A09	NC
30	GND	A01	IRQ1*	A08	+3.3V
31	NC	-12V	NC	+12V	GND
32	GND	+5V	+5V	+5V	+5V

Table 11 VME P1 Pinout

7.3. VME P2

Pin	Row z	Row a	Row b	Row c	Row d
1	PMC_J14-2	PMC_J24-2	+5V	PMC_J24-1	PMC_J14-1
2	GND	PMC_J24-4	GND	PMC_J24-3	PMC_J14-3
3	PMC_J14-5	PMC_J24-6	NC	PMC_J24-5	PMC_J14-4
4	GND	PMC_J24-8	A24	PMC_J24-7	PMC_J14-6
5	PMC_J14-8	PMC_J24-10	A25	PMC_J24-9	PMC_J14-7
6	GND	PMC_J24-12	A26	PMC_J24-11	PMC_J14-9
7	PMC_J14-11	PMC_J24-14	A27	PMC_J24-13	PMC_J14-10
8	GND	PMC_J24-16	A28	PMC_J24-15	PMC_J14-12
9	PMC_J14-14	PMC_J24-18	A29	PMC_J24-17	PMC_J14-13
10	GND	PMC_J24-20	A30	PMC_J24-19	PMC_J14-15
11	PMC_J14-17	PMC_J24-22	A31	PMC_J24-21	PMC_J14-16
12	GND	PMC_J24-24	GND	PMC_J24-23	PMC_J14-18
13	PMC_J14-20	PMC_J24-26	+5V	PMC_J24-25	PMC_J14-19
14	GND	PMC_J24-28	D16	PMC_J24-27	PMC_J14-21
15	PMC_J14-23	PMC_J24-30	D17	PMC_J24-29	PMC_J14-22
16	GND	PMC_J24-32	D18	PMC_J24-31	PMC_J14-24
17	PMC_J14-26	PMC_J24-34	D19	PMC_J24-33	PMC_J14-25
18	GND	PMC_J24-36	D20	PMC_J24-35	PMC_J14-27
19	PMC_J14-29	PMC_J24-38	D21	PMC_J24-37	PMC_J14-28
20	GND	PMC_J24-40	D22	PMC_J24-39	PMC_J14-30
21	PMC_J14-32	PMC_J24-42	D23	PMC_J24-41	PMC_J14-31
22	GND	PMC_J24-44	GND	PMC_J24-43	PMC_J14-33
23	PMC_J14-35	PMC_J24-46	VD24	PMC_J24-45	PMC_J14-34
24	GND	PMC_J24-48	VD25	PMC_J24-47	PMC_J14-36
25	PMC_J14-38	PMC_J24-50	VD26	PMC_J24-49	PMC_J14-37
26	GND	PMC_J24-52	VD27	PMC_J24-51	PMC_J14-39
27	PMC_J14-41	PMC_J24-54	VD28	PMC_J24-53	PMC_J14-40
28	GND	PMC_J24-56	VD29	PMC_J24-55	PMC_J14-42
29	PMC_J14-44	PMC_J24-58	VD30	PMC_J24-57	PMC_J14-43
30	GND	PMC_J24-60	VD31	PMC_J24-59	PMC_J14-45
31	PMC_J14-46	PMC_J24-62	GND	PMC_J24-61	GND
32	GND	PMC_J24-64	+5V	PMC_J24-63	+5V

Table 12 VME P2 Pinout

7.4. Jx1, Jx2 PMC Connectors

Jx1 32 Bit PCI				Jx2 32 Bit PCI			
Pin	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**
1	TCK	-12V	2	1	+12V	TRST#	2
3	Ground	INTA#	4	3	TMS	TDO	4
5	INTB#	INTC#	6	5	TDI	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	NC	8

9	INTD#	NC	10	9	NC	NC	10
11	Ground	NC	12	11	BUSMODE2#	+3.3V	12
13	CLK	Ground	14	13	RST#	BUSMODE3#	14
15	Ground	GNT#	16	15	3.3V	BUSMODE4#	16
17	REQ#	+5V	18	17	PME#	Ground	18
19	V(I/O)	AD[31]	20	19	AD[30]	AD[29]	20
21	AD[28]	AD[27]	22	21	Ground	AD[26]	22
23	AD[25]	Ground	24	23	AD[24]	+3.3V	24
25	Ground	C/BE[3]#	26	25	IDSEL	AD[23]	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28
29	AD[19]	+5V	30	29	AD[18]	Ground	30
31	V(I/O)	AD[17]	32	31	AD[16]	C/BE[2]#	32
33	FRAME#	Ground	34	33	Ground	IDSELB	34
35	Ground	IRDY#	36	35	TRDY#	+3.3V	36
37	DEVSEL#	+5V	38	37	Ground	STOP#	38
39	PCIXCAP	LOCK#	40	39	PERR#	Ground	40
41	NC	NC	42	41	+3.3V	SERR#	42
43	PAR	Ground	44	43	C/BE[1]#	Ground	44
45	V(I/O)	AD[15]	46	45	AD[14]	AD[13]	46
47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48
49	AD[09]	+5V	50	49	AD[08]	+3.3V	50
51	Ground	C/BE[0]#	52	51	AD[07]	REQB#	52
53	AD[06]	AD[05]	54	53	+3.3V	GNTB#	54
55	AD[04]	Ground	56	55	NC	Ground	56
57	(I/O)	AD[03]	58	57	NC	NC	58
59	AD[02]	AD[01]	60	59	Ground	NC	60
61	AD[00]	+5V	62	61	ACK64#	+3.3V	62
63	Ground	REQ64#	64	63	Ground	MONARCH#	64

Notes:
V(I/O) = 3.3V
For signal definitions, see IEEE Std 1386-2001

Table 13 Jx1, Jx2 Connector Pinout

7.5. Jx3, Jx4 PMC Connectors

Jx3 64 Bit PCI				Jx4 User Defined I/O			
Pin	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**
1	NC	Ground	2	1	I/O	I/O	2
3	Ground	C/BE[7]#	4	3	I/O	I/O	4
5	C/BE[6]#	C/BE[5]#	6	5	I/O	I/O	6
7	C/BE[4]#	Ground	8	7	I/O	I/O	8
9	V(I/O)	PAR64	10	9	I/O	I/O	10
11	AD[63]	AD[62]	12	11	I/O	I/O	12
13	AD[61]	Ground	14	13	I/O	I/O	14
15	Ground	AD[60]	16	15	I/O	I/O	16
17	AD[59]	AD[58]	18	17	I/O	I/O	18
19	AD[57]	Ground	20	19	I/O	I/O	20
21	V(I/O)	AD[56]	22	21	I/O	I/O	22
23	AD[55]	AD[54]	24	23	I/O	I/O	24
25	AD[53]	Ground	26	25	I/O	I/O	26
27	Ground	AD[52]	28	27	I/O	I/O	28
29	AD[51]	AD[50]	30	29	I/O	I/O	30
31	AD[49]	Ground	32	31	I/O	I/O	32
33	Ground	AD[48]	34	33	I/O	I/O	34
35	AD[47]	AD[46]	36	35	I/O	I/O	36
37	AD[45]	Ground	38	37	I/O	I/O	38
39	V(I/O)	AD[44]	40	39	I/O	I/O	40
41	AD[43]	AD[42]	42	41	I/O	I/O	42
43	AD[41]	Ground	44	43	I/O	I/O	44
45	Ground	AD[40]	46	45	I/O	I/O	46
47	AD[39]	AD[38]	48	47	I/O	I/O	48
49	AD[37]	Ground	50	49	I/O	I/O	50

51	Ground	AD[36]	52	51	I/O	I/O	52
53	AD[35]	AD[34]	54	53	I/O	I/O	54
55	AD[33]	Ground	56	55	I/O	I/O	56
57	V(I/O)	AD[32]	58	58	I/O	I/O	58
59	NC	NC	60	59	I/O	I/O	60
61	NC	Ground	62	61	I/O	I/O	62
63	Ground	NC	64	63	I/O	I/O	64

Notes:
V(I/O) = 3.3V
For signal definitions, see IEEE Std 1386-2001

Table 14 Jx3, Jx4 Connector Pinout

7.6. Jx5 XMC Primary Connector

	A	B	C	D	E	F
01	DP00+	DP00-	3.3V	DP01+	DP01-	VPWR
02	GND	GND	NC	GND	GND	MRSTI#
03	DP02+	DP02-	3.3V	DP03+	DP03-	VPWR
04	GND	GND	NC	GND	GND	MRSTO#
05	DP04+	DP04-	3.3V	DP05+	DP05-	VPWR
06	GND	GND	NC	GND	GND	+12V
07	DP06+	DP06-	3.3V	DP07+	DP07-	VPWR
08	GND	GND	NC	GND	GND	-12V
09	NC	NC	NC	NC	NC	VPWR
10	GND	GND	NC	GND	GND	GA0
11	DP10+	DP10-	NC	DP11+	DP11-	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	DP12+	DP12-	NC	DP13+	DP13-	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	DP14+	DP14-	NC	DP15+	DP15-	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	DP16+	DP16-	NC	DP17+	DP17-	NC
18	GND	GND	NC	GND	GND	NC
19	REFCLK +	REFCLK-	NC	PCIE_WAKE	PCIE_ROOT	NC

Notes:
VPWR = 5.0V
JTAG Connections pulled high to inactive state and TDI is connected to TDO.
For signal definitions, see VITA42.0, VITA42.2 (Serial Rapid IO) or VITA42.3 (PCI-Express)

Table 15 Jx5 Connector Pinout

7.7. Jx6 XMC Secondary Connector

	A	B	C	D	E	F
01	DP00+	DP00-	NC	DP01+	DP01-	NC
02	GND	GND	NC	GND	GND	NC
03	DP02+	DP02-	NC	DP03+	DP03-	NC
04	GND	GND	NC	GND	GND	NC
05	DP04+	DP04-	NC	DP05+	DP05-	NC
06	GND	GND	NC	GND	GND	NC
07	DP06+	DP06-	NC	DP07+	DP07-	NC
08	GND	GND	NC	GND	GND	NC
09	NC	NC	NC	NC	NC	NC
10	GND	GND	NC	GND	GND	NC
11	DP10+	DP10-	NC	DP11+	DP11-	NC
12	GND	GND	NC	GND	GND	NC
13	DP12+	DP12-	NC	DP13+	DP13-	NC
14	GND	GND	NC	GND	GND	NC
15	DP14+	DP14-	NC	DP15+	DP15-	NC
16	GND	GND	NC	GND	GND	NC
17	DP16+	DP16-	NC	DP17+	DP17-	NC
18	GND	GND	NC	GND	GND	NC
19	NC	NC	NC	NC	NC	NC

Table 16 Jx6 Connector Pinout

7.8. J1 JTAG Connector

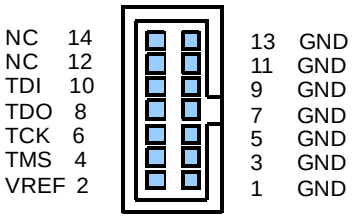

Figure 6 JTAG Connector J1 Pinout

For use with Xilinx Parallel IV or Platform Cable USB IDC ribbon cables. For more information see DS300 or DS097 available at www.xilinx.com.

7.9. J11 / J12 JTAG Headers

J11 is located near PMC #2, J12 is located near PMC #1.

Pin	Function
1	VCC (JTAG I/O Voltage input from Mezzanine Card)
2	GND
3	Unused
4	TCK
5	NC
6	TDO
7	TDI
8	*KEY* Not Installed
9	TMS

Table 17 JTAG Headers (To Mezzanine Cards) Pinout

8. Revision History

Date	Revision	Nature of Change
11/06/08	1.0	Created user manual
11/17/10	1.1	Clarified Table 1, SW3 had polarity documented incorrectly