ALPHA DATA

ADM-PCIE-7V3
User Manual

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1 Introduction

The ADM-PCIE-7V3 is a high-performance reconfigurable computing card intended for Data Center applications, featuring a Xilinx Virtex-7 FPGA.

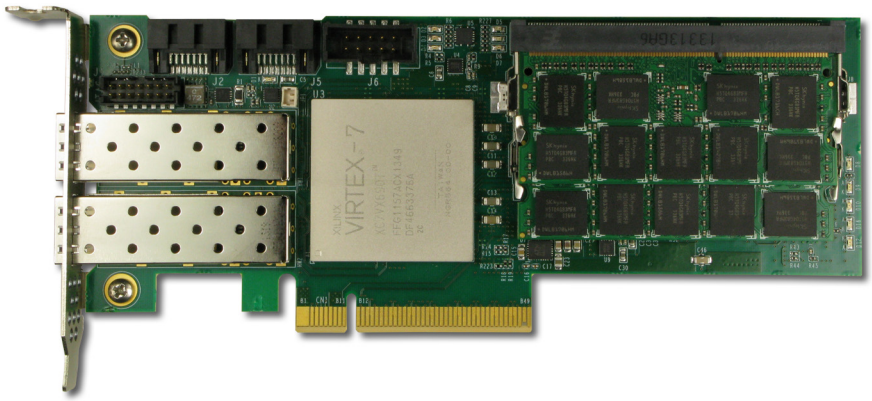

Figure 1 : ADM-PCIE-7V3 Product Photo

1.1 Key Features

Key Features

- Compatible with Xilinx OpenCL compiler
- Supported by ADM-XRC Gen 3 SDK 1.7.0 or later and ADB3 Driver 1.4.15 or later.
- PCIe Gen1/2/3 x1/2/4/8 capable
- Half-length, low-profile x8 PCIe form factor
- Two banks of DDR3 SDRAM SODIMM memory with ECC, rated at 1333MT/s
- Two right angle SATA connectors (SATA3 capable)
- Two SFP+ sites capable of data rates up to 10 Gbps
- FPGA configurable over JTAG and BPI Flash
- XC7VX690T-2FFG1157C FPGA
- Voltage, current, and temperature monitoring

1.2 Order Code

ADM-PCIE-7V3/VX690T-2

2 PCB Information

2.1 Physical Specifications

The ADM-PCIE-7V3 complies with PCI Express CEM revision 3.0.

Description	Measure
Total Dy	68.9 mm
Total Dx (Inc. SFP+ Cages)	174.5 mm
Total Dz	32.5 mm
Weight	120 g

Table 1 : Mechanical Dimensions

2.2 Chassis Requirements

2.2.1 PCI Express

The ADM-PCIE-7V3 is capable of PCIe Gen 1/2/3 with 1/2/4/8 lanes, using the Xilinx Integrated Block for PCI Express.

2.2.2 Mechanical Requirements

An 8-lane or 16-lane physical PCIe slot is required for mechanical compatibility.

Each ADM-PCIE-7V3 is shipped with a full height PCIe card bracket attached. Each shipment also contains a low-profile PCIe card bracket so that users with a low-profile chassis can replace the card bracket in order to suit their chassis.

Because most PC chassis do not provide sufficient airflow to cool the FPGA, the ADM-PCIE-7V3 is shipped with a fan on the heatsink. This fan and heatsink assembly consumes part of the adjacent PCIe slot, so the cards must have an unpopulated PCIe slot between them.

If sufficient airflow is available, the fan can be removed so that the ADM-PCIE-7V3 can be placed immediately adjacent to a populated PCIe slot. This requires that the ADM-PCIE-7V3 is only adjacent to other ADM-PCIE-7V3 cards, and that the system provides sufficient airflow to keep the FPGA of the ADM-PCIE-7V3 below 85 degrees Celsius.

2.2.3 Power Requirements

NOTE
By default, SODIMM and SFP power supplies are disabled.

The PCIe Specification permits a standard low-profile, half-length PCIe card to dissipate up to 25 W of power, drawn from the PCIe slot. The ADM-PCIE-7V3 may consume more than 25 W of power for worst-case user FPGA designs. Power estimation requires the use of the Xilinx XPE spreadsheet and/or a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

To save power, certain power supplies that are not required by all FPGA designs are disabled on power-up. To enable these supplies, drive the corresponding enable pin high ('1'):

Power Supply	Description	FPGA Pin
3V3_SFP	SFP+ Front Panel I/O Power Supply	AA23
1V5_DRAM	DDR3 SDRAM SODIMM Power Supply	AA24

Table 2 : Power Supply Enables

There are two options to confirm that a power supply has been enabled and is operating properly. First, the user can check illumination of the LED power indicators (see LEDs). Additionally, the state of the Power OK pins at the FPGA can be checked. A logical '1' at the pins in the table below indicates that the supply voltage is operating within tolerance.

Power Supply	Description	FPGA Pin
3V3_SFP	SFP+ Front Panel I/O Power Supply	W30
1V5_DRAM	DDR3 SDRAM SODIMM Power Supply	AA31

Table 3 : Power OK Pins

Whe using an interface that was initially powered down at startup, logically AND the Power OK signal with the interface reset to ensure that all communication attempts occur after power is stable.

NOTE
As a precaution against latchup-type phenomena, do not power down the SFP+ Power Supply if the FPGA drives any of its pins related to SFP+ functionality. Similarly, do not power down the DDR3 SDRAM SODIMM power supply if the FPGA drives any of its pins related to DDR3 SDRAM functionality.

2.2.4 VCC_INT Limits

For ADM-PCIE-7V3 designs should limit the VCC_INT usage as shown in the table below. If this limit is exceeded the VCC_INT voltage may drop below the FPGA recommended range. While the FPGA may continue to function nominally at higher current draws, this is not recommended. For SN 319 and newer, if the current on VCC_INT reaches 30A the board will power down to protect from damaging onboard components.

Serial Range	VCC_INT Limit
100-318	14A
319 and higher	22A

Table 4 : VCC_INT Limits

2.3 Thermal Characterization

The theta junction-to-ambient (Theta-JA) for the FPGA as related to air flow in linear feet per minute (LFM) is specified in the graph below. Use the Xilinx Power Estimator (XPE) to determine the expected power of your FPGA design (http://www.xilinx.com/products/design_tools/logic_design/xpe.htm)

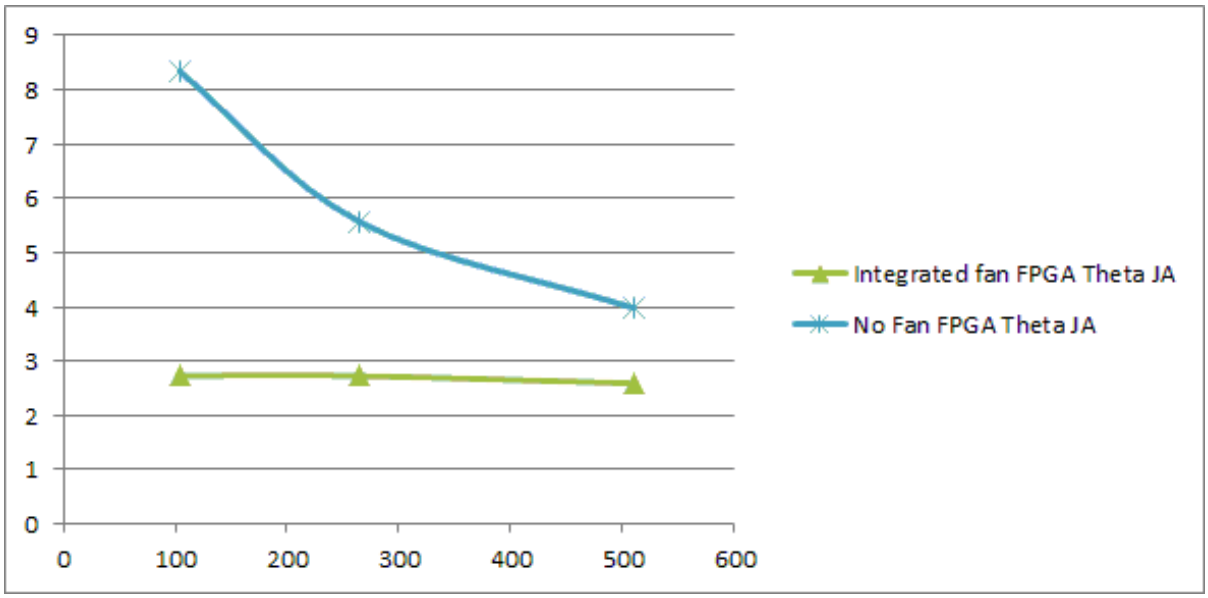

Figure 2 : FPGA Theta-JA vs LFM

3 Functional Description

3.1 Overview

The ADM-PCIE-7V3 is a versatile reconfigurable computing platform with a Virtex-7 VX690T-2 FPGA, a Gen3x8 PCIe interface, two slots for DDR3-1333 SDRAM SODIMMs (64 bits with 8 bits ECC), two SFP+ cages capable of 10G Ethernet, two SATA3 connectors, and a robust system monitor.

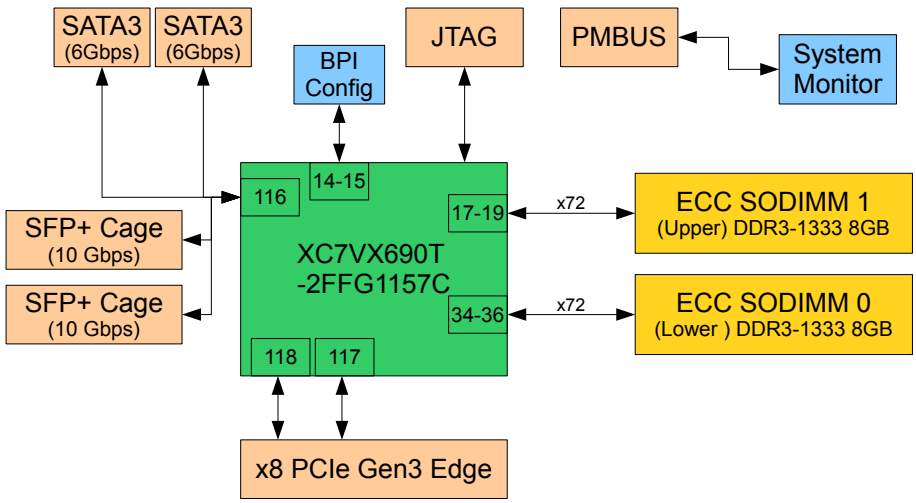

Figure 3 : ADM-PCIE-7V3 Block Diagram

3.1.1 Switches

The ADM-PCIE-7V3 has a quad DIP switch SW1, located on the rear side of the board near the card bracket. The function of each switch in SW1 is detailed below:

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	Xilinx/AD Mode	Configure from Alpha Data region	Configure from Xilinx region
SW1-2	ON	Flash Lockdown	Flash block Lockdown enabled	Flash block Lockdown disabled
SW1-3	ON	Failsafe/ Default	Configure from failsafe region	Configure from default region
SW1-4	OFF	User Switch	Pin AB30 = '1'	Pin AB30 = '0'

Table 5 : SW1 Switch Functions

3.1.2 LEDs

There are 12 LEDs on the ADM-PCIE-7V3, 6 of which are general purpose and whose meaning can be defined by the user. The other five have fixed functions such as power supply status and the configuration status of the FPGA.

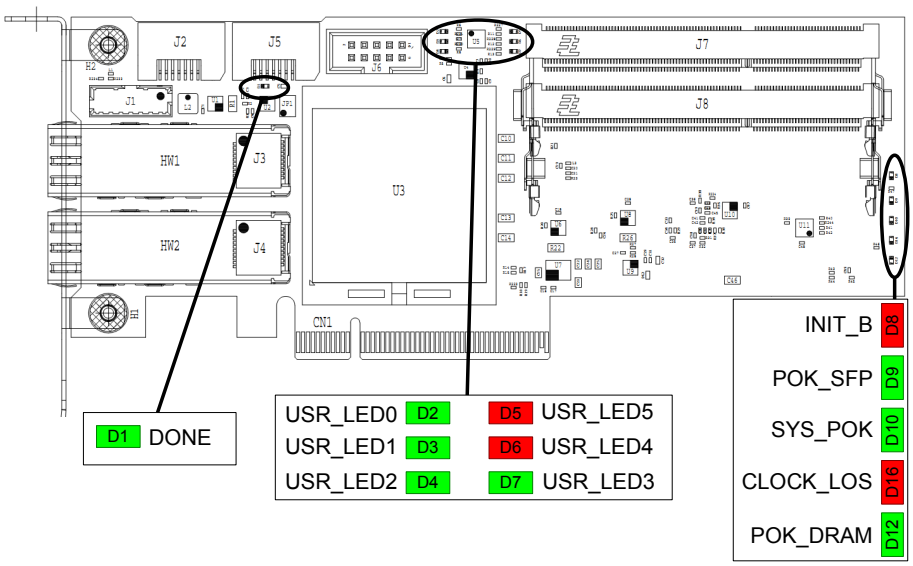

Figure 4 : LEDs

Comp. Ref.	Function	ON State	OFF State
D1	DONE	FPGA is configured	FPGA is not configured
D2	USR_LED0	User defined '1' pin AC33	User defined '0' pin AC33
D3	USR_LED1	User defined '1' pin V32	User defined '0' pin V32
D4	USR_LED2	User defined '1' pin V33	User defined '0' pin V33
D5	USR_LED5	User defined '1' pin U30	User defined '0' pin U30
D6	USR_LED4	User defined '1' pin AB32	User defined '0' pin AB32
D7	USR_LED3	User defined '1' pin AB31	User defined '0' pin AB31
D8	INIT_B	Error during configuration	No error during configuration
D9	POK_SFP	SFP+ power supply OK	SFP+ power supply OFF or out of range
D10	SYS_POK	All FPGA power rails OK	One or more FPGA power rails out of range
D12	POK_DRAM	SODIMM power supply OK	SODIMM power supply OFF or out of range
D16	CLOCK_LOS	Clocks not operating normally	Clocks operating normally

Table 6 : LED Details

3.2 Clocking

The ADM-PCIE-7V3 provides reference clocks for the DDR3 SDRAM banks and the I/O interfaces available to the user.

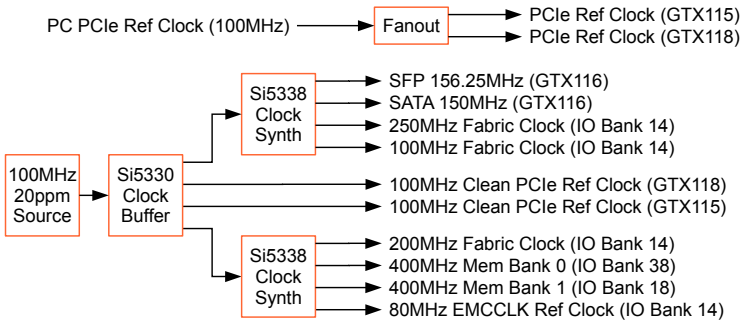

Figure 5 : Clock Topology

3.2.1 PCIe Reference Clocks

The 8 MGT lanes connected to the PCIe card edge use MGT tiles 117 and 118. There are two clocking options available: (i) the internally generated 100 MHz reference clock with a tight 20 ppm tolerance (REFCLK100M_5), and (ii) the system 100 MHz clock (PCIE_REFCLK1).

The other reference clocks (PCIE_REFCLK0 and REFCLK100M_4) are connected to a unused MGT tiles and can be used for fabric clocking.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
PCIE_REFCLK1	MGTREFCLK0_118	LVDS	F6	F5
REFCLK100M_5	MGTREFCLK1_118	LVDS	H6	H5
PCIE_REFCLK0	MGTREFCLK0_115	LVDS	AB6	AB5
REFCLK100M_4	MGTREFCLK1_115	LVDS	AD6	AD5

Table 7 : PCIe Reference Clocks

3.2.2 Fabric Clocks

The design offers 3 fabric clocks: REFCLK200M is a 200 MHz clock intended to be used for IDELAY elements in FPGA designs. REFCLK100M and REFCLK250M run at 100 MHz and 250 MHz respectively and can be used to drive internal PLLs and other clocking resources. Each fabric clock is connected to a Multi-Regional Clock Capable (MRCC) pin.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
REFCLK200M	IO_L13_T2_MRCC_15	LVDS	AD29	AE29
REFCLK100M_8	IO_L12_T1_MRCC	LVDS	AE31	AF31
REFCLK250M	IO_L12_T1_MRCC_14	LVDS	AL29	AL30

Table 8 : Fabric CLocks

3.2.3 Programming Clock (EMCCLK)

An 80MHz clock is fed into the EMCCLK pin to drive the BPI flash device during configuration of the FPGA.

Signal	Target FPGA Input	I/O Standard	pin
REFCLK80M	IO_L3N_T0_DQS_EMCCLK_14	1V8_CMOS	AP33

Table 9 : EMCCLK

3.2.4 Cabled HSSIO (SFP+/SATA)

The SATA and SFP+ cages share MGT tile 116. The reference clocks for both the SATA and SFP+ interfaces are input into the FPGA at this tile.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
REFCLK156M25	MGTREFCLK0_116	LVDS	T6	T5
REFCLK150M	MGTREFCLK1_116	LVDS	V6	V5

Table 10 : SFP+ and SATA Reference Clocks

3.2.5 DDR3 SDRAM Reference Clocks

The two banks of DDR3 SDRAM memory each require a separate reference clock, as per Xilinx Virtex-7 MIG design guidelines. The reference clocks for these interfaces are detailed below:

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
REFCLK400M_0	IO_L12_T1_MRCC_35	HSTL	AH15	AJ15
REFCLK400M_1	IO_L12_T1_MRCC_18	HSTL	G30	G31

Table 11 : Memory Reference Clocks

3.3 PCI Express

The ADM-PCIE-7V3 is capable of PCIe Gen 1/2/3 with 1/2/4/8 lanes. The FPGA drives these lanes directly using the Integrated PCI Express block from Xilinx. Negotiation of PCIe link speed and number of lanes used is generally automatic and does not require user intervention.

PCI Express reset (PERST#) is buffered, level shifted, and connected to the FPGA at pin W27.

The other pin assignments for the high speed lanes are provided in the table below:

Signal	Target FPGA Input	P pin	N pin
PCIE_TX0	MGTHTX3_118	A4	A3
PCIE_RX0	MGTHRX3_118	B6	B5
PCIE_TX1	MGTHTX2_118	B2	B1
PCIE_RX1	MGTHRX2_118	D6	D5
PCIE_TX2	MGTHTX1_118	C4	C3
PCIE_RX2	MGTHRX1_118	E4	E3
PCIE_TX3	MGTHTX0_118	D2	D1
PCIE_RX3	MGTHRX0_118	G4	G3
PCIE_TX4	MGTHTX3_117	F2	F1
PCIE_RX4	MGTHRX3_117	J4	J4
PCIE_TX5	MGTHTX2_117	H2	H1
PCIE_RX5	MGTHRX2_117	K6	K5
PCIE_TX6	MGTHTX1_117	K2	K1
PCIE_RX6	MGTHRX1_117	L4	L3
PCIE_TX7	MGTHTX0_117	M2	M1
PCIE_RX7	MGTHRX0_117	N4	N3

Table 12 : PCI Express Pin Assignments

3.4 DDR3 SDRAM SODIMMs

Two DDR3 SDRAM SODIMM connectors can accommodate up to two SODIMMs with 72-bit wide data (64 data + 8 ECC). Maximum signaling rate is 1333 MT/s, and maximum memory capacity is 8 GiB per SODIMM. Peak theoretical memory bandwidth for both banks combined is approximately 165 Gbps.

Memory solutions are available from the Xilinx Memory Interface Generator (MIG) tool. Both the Xilinx OpenCL development tools and the ADM-XRC Gen 3 SDK include memory interface examples and constraint files for reference when implementing a new FPGA design.

3.5 SFP+

Two SFP+ cages are available at the front panel. Both cages are capable of housing either active optical or passive copper SFP+ compatible components. The communication interface can run at speeds capable of handing 10G Ethernet or any other protocol supported by the Xilinx MGT Transceivers. Please see Xilinx User Guide UG476 for more details on the capabilities of the transceivers.

If the SFP+ cages are unused, or using copper cabling, it is recommended that the 3.3V power supply for the transceivers is disabled to save power. Please see Power Requirements for more details.

Both SFP+ cages have all control signals connected to the FPGA. Their connectivity is described in the table below. The I/O standard used by these pins is LVCMOS18.

Signal J4(HW2)	iPass Pin	FPGA Pin	|	FPGA Pin	iPass Pin	Signal J3(HW1)
SFP+0_TX_FAULT	2	Y33	|	V34	2	SFP+1_TX_FAULT
SFP+0_TX_DISABLE	3	AC34	|	AA34	3	SFP+1_TX_DISABLE
SFP+0_SDA	4	Y29	|	V28	4	SFP+1_SDA
SFP+0_SCL	5	V27	|	V29	5	SFP+1_SCL
SFP+0_MOD_ABS	6	W34	|	V23	6	SFP+1_MOD
SFP+_RS0	7	Y34*	|	Y34*	7	SFP+_RS0
SFP+_RS1	9	AC32*	|	AC32*	9	SFP+_RS1
SFP+01_LOS	8	AB33	|	AA33	8	SFP+1_LOS

Table 13 : SFP+ Control Signals

Note:
SFP+0/1_TX_DISABLE is pulled up be default and must be driven low to enable most optical modules.
*The rate select pins are connected in parallel between the cages

The data path for the two modules is shown in the table below:

Ref. Des.	Signal	Target FPGA Input	P pin	N pin
J4(HW2)	SFP+_TX0	MGTHTX2_116	T2	T1
J4(HW2)	SFP+_RX0	MGTHRX2_116	U4	U3
J3(HW1)	SFP+_TX1	MGTHTX3_116	P2	P1
J3(HW1)	SFP+_RX1	MGTHRX3_116	R4	R3

Table 14 : SFP+ Transceiver Signals

3.6 SATA

Two SATA receptacles along the top of the board allow for internal chassis SATA management. The SATA interface can support the third generation SATA specification operating at 6 Gbps. Alpha Data can provide IP to manage the SATA devices connected at this interface. Please contact sales@alpha-data.com for more information regarding SATA IP.

Both RX and TX lines are AC coupled with 10nF capacitors. The pin assignments for this interface are detailed below:

Ref. Des.	Signal	Target FPGA Input	P pin	N pin
J2	SATA_TX0	MGTHTX0_116	Y2	Y1
J2	SATA_RX0	MGTHRX0_116	AA4	AA3
J5	SATA_TX1	MGTHTX1_116	V2	V1
J5	SATA_RX1	MGTHRX1_116	W4	W3

Table 15 : SATA Signals

3.7 System Monitor

System Monitor Fault Responses
TI Fusion Communication Components
All power rails are sequenced and monitored by a system monitor IC. The device used in this design is a TI Fusion UCD90120A. The TI Fusion controller monitors certain voltage readings, current readings, and Power OK signals to determine the state of the system. D10 SYS_POK lights if all values are nominal (see Section LEDs for LED Location).

If the system monitor detects an inappropriate voltage, temperature, or current, it takes the following actions:

- FPGA Core Temperature above operating max (85 degC): Reconfigure FPGA from failsafe region.
- Voltage rail outside recommended values in Virtex 7 Datasheet (DS183): Log Fault
- Voltage rail outside maximums specified Virtex 7 Datasheet (DS183): Power down board.
- Rail current exceeds supply maximum: Power down board.

A PC can directly interact with the TI Fusion IC via the PMBUS header in the design. This requires the following items:

- Programing Box: TI part number "USB-TO-GPIO"
- TI Digital Power Designer software (http://www.ti.com/tool/fusion_digital_power_designer)
- xml configuration file from Alpha Data (contact support@alpha-data.com)

3.8 Configuration

There are two main ways of configuring the FPGA on the ADM-PCIE-7V3:

- From Flash memory, at power-on, as described in Section 3.8.1
- Using a Xilinx JTAG platform cable connected to J1, as described in Section 3.8.2

3.8.1 Configuration From Flash Memory

The FPGA can be automatically configured at power-on from a 1 Gbit BPI flash memory device (Micron part number PC28F00AG18). This Flash device is divided into four regions of 32 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for a 7VX690T FPGA.

The ADM-PCIE-7V3 is shipped with a bitstream, corresponding to the "simple" FPGA design from the ADM-XRC Gen 3 SDK, programmed into regions 0 and 1. This permits basic confidence testing to be performed on a board without needing to program anything into the Flash memory. Alpha Data recommends that region 0 is never overwritten; this permits relatively simple recovery, without requiring a Xilinx Platform USB JTAG cable to be attached, in the event of programming a "bad" bitstream into region 1.

The flash address map is as detailed below:

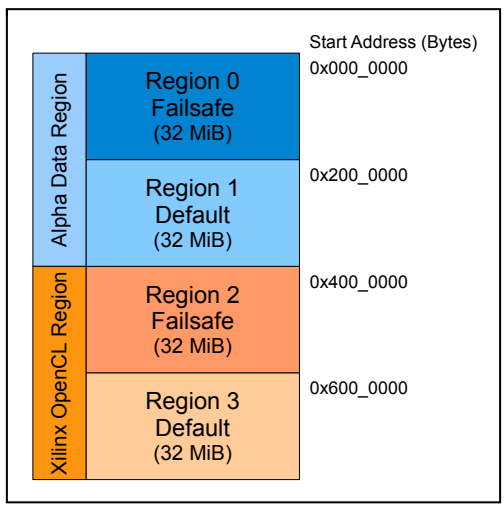

Figure 6 : Flash Address Map

At power-on, the FPGA attempts to configure itself automatically in BPI mode from one of the four regions of the Flash, determined by SW1-1 and SW-3 (see Section 3.1.1) as follows:

SW1-1	SW1-3	Region used for configuration
OFF	OFF	0
OFF	ON	1 (factory default)
ON	OFF	2
ON	ON	3

Table 16 : Flash Configuration Region Selection

The Lockdown function of the Flash device is controlled via switch SW1-2. When SW1-2 is ON, any blocks in the Flash whose Lockdown flag is set are write-protected. The factory default for the Lockdown flag of all Flash blocks is clear, so that any block in the Flash can be written.

3.8.1.1 Building Configuration Images

Generate a bitfile with these constraints (see XAPP587):

- set_property BITSTREAM.GENERAL.COMPRESS {TRUE} [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-1} [current_design]
- set_property BITSTREAM.CONFIG.BPI_SYNC_MODE {TYPE1} [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property BITSTREAM.CONFIG.BPI_PAGE_SIZE {1} [current_design]
- set_property BITSTREAM.CONFIG.CONFIGRATE {3} [current_design]
- set_property CONFIG_MODE {BPI16} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 128
- -interface BPIx16
- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (failsafe location)
- -loadbit "up 0x1000000 <directory/to/file/filename.bit>" (default location)

Program with vivado hardware manager with these settings:

- BPI part number: mt28gu01gaax1e-bpi-x16
- RS bits: 25:24

3.8.2 Configuration via JTAG

A Xilinx Platform USB Cable may be attached to connector J1. This permits the FPGA to be reconfigured using the IMPACT tool from Xilinx ISE, or using the Xilinx Vivado Hardware Manager.

Revision History

Date	Revision	Changed By	Nature of Change
7th May 2014	0.1	K. Roth	Initial Draft
9th May 2014	1.0	K. Roth	Initial Release
28th May 2014	1.1	K. Roth	Changed all references to DDR3 speed to DDR3-1333
27th Aug 2014	1.2	K. Roth	Modified Power Requirements to include POK pin table and accurate description of power states at power-on.
4th May 2015	1.3	K. Roth	Added Thermal Characterization and VCC_INT Limits
3rd June 2016	1.4	K. Roth	Added note in SFP+ about rate select being shared, updated image in Introduction, correction reference designation of programming connector in Configuration, added Building Configuration Images

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