Alpha Data LZ77 Compression Card : ADM-PCIE-KU3-LZ77

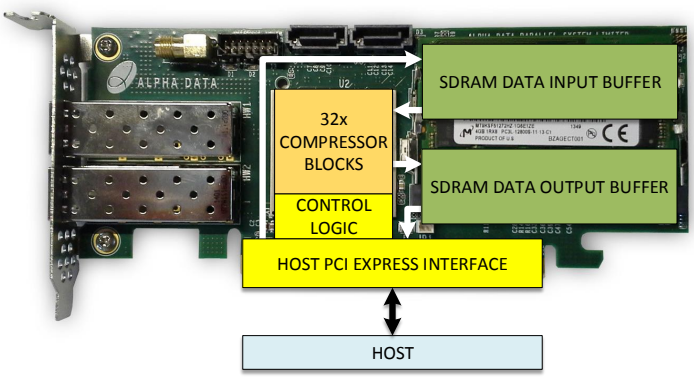
ADM-PCIE-KU3, low profile PCIE Data centre FPGA Card, with LZ Compression IP core provided by Helion Technology Limited - http://www.heliontech.com

ADM-PCIE-KU3 Technical Specification:

- Board Format : Half-Length, low profile x16 PCIe form factor
- Host I/F : PCI Express® Gen3 x8 (supports 2nd x8 PCIE hard macro or soft x16 cores)
- Target Device : Xilinx® Kintex® Ultrascale™ : XCKU060 - FFVA1156
- ECC-SODIMM : Two 8GB DDR3 ECC-SODIMM for memory speeds up to 1600MT/s
- FLASH : 1GBit of BPI x 16 configuration flash
- Dual QSFP+ cages for high speed optical comms including 10 and 40 Gig Ethernet
- Dual SATA Interfaces

About Helion Compression Cores

The Helion Compression cores provide high-performance, resource efficient lossless data compression solutions for accelerating a range of algorithms based on the Lempel-Ziv 1977 (LZ77) compression methods without the need for off-chip memory. Supported algorithms include static Huffman coding based compression which give enhanced compression results, as well as compatibility with widely used software compression algorithms, such as DEFLATE.



The Helion Cores are ideal for improving system performance and efficiency in a variety of data communications, networking and data storage applications. The cores can be supplied in Compress only, Decompress only or Compress/Decompress versions to suit any design requirement. Each Compression Core is capable of handling data rates up to 2 Gbps in Xilinx FPGA devices which can easily be scaled up to implement very high data throughput compression solutions using multiple cores. In the Alpha Data Compression Card, 32 Helion LZ77 Cores can provide up to 5.8GB/s compression capability, matched to host PCIe bandwidth and on-board DDR3 memory bandwidth.

Comparison

System	Design	Compression Ratio[1] [2]	Rate	Description
FPGA	Helion LZ77	49%	~5.1GB/s	for 32 cores @ 200MHz
x86	Snappy	49%[3]	~300MB/s[4]	single thread, i5-3340 @ 2.7GHz
x86	LZ4 (-1)	38%[3]	~400MB/s[4]	single thread, i5-3340 @ 2.7GHz
x86	Zlib/DEFLATE (-6)	32%[3]	~20MB/s[4]	single thread, i5-3340 @ 2.7GHz

Notes:
1 - Compression ratio is the output size as a percentage of the original size
2 - source : http://sun.aei.polsl.pl/~sdeor/index.php?page=silesia
3 - Source : http://mattmahoney.net/dc/silesia.html
4 - Source : http://lz4.github.io/lz4/

The Compression card is provided with Alpha Data Host API and Driver, compatible with Windows and Linux.

Estimated FPGA Resource Utilisation

FPGA	CLBs	Registers	BRAM Memory	DSPs
Xilinx Kintex Ultrascale XCKU060 - FFVA1156	331,680	663,360	38Mb	2260
32 LZ77 Core System[1]	65%	45%	40%	5%

Notes:
1 - These figures include the PCI Express and Memory Interfaces as well as board monitoring logic

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