ALPHA DATA

ADM-VPX3-9Z2
User Manual

Document Revision: 1.1
16th January 2020

	Head Office	US Office
Address:	Suite L4A, 160 Dundee Street, Edinburgh, EH11 1DQ, UK	611 Corporate Circle, Suite H Golden, CO 80401
Telephone:	+44 131 558 2600	(303) 954 8768
Fax:	+44 131 558 2700	(866) 820 9956 - toll free
email:	sales@alpha-data.com	sales@alpha-data.com
website:	http://www.alpha-data.com	http://www.alpha-data.com

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1 Introduction

The **ADM-VPX3-9Z2** shall be a high performance reconfigurable 3U OpenVPX format board based on the Xilinx Zynq Ultrascale+ range of Multiprocessor System-on-Chips (MPSoC).

1.1 Key Features

Key Features

- 3U Open VPX, compliant to VITA Standard 46.0 and 65
- FMC+ interface compliant to Vita 57.4 with high density connector
- Support for Zynq Ultrascale+ ZU9/ZU15 MPSoC in FFVB1156 package
- VPX P1 utilized according to OpenVPX payload slot profile SLT3-PAY-1F1F2U-14.2.4
- 4 optical duplex lanes at data rates of up to 10Gbps as described in Vita 66.4
- Half width P2 with 24 GPIO as described in Vita 66.4
- Processing System (PS) Block consisting of:
  - Quad-core ARM Cortex-A53, Dual-core ARM Cortex-R5, Mali-400 GPU
  - 1 bank of DDR4-2400 SDRAM, 1GB x72, 8GB total + ECC
  - Removable microSD Flash memory
  - Two Quad SPI Flash memory, up to 2Gb each
  - Two USB ports to VPX P1
- Programmable Logic (PL) block consisting of:
  - 600k logic cells (ZU9EG) or 747k logic cells (ZU15EG)
- 4-lanes of HSSIO on the PS block that can be configured as either:
  - Dedicated 4 lane PCI-Express Gen 2 interface on the OpenVPX Data Plane
  - 3 lanes on the OpenVPX Expansion Plane and 1 lane to an on board SSD drive chip
  - 1 lane of PCIe on the Data Plane, 2 lanes on the Expansion Plane and 1 lane to the mSATA socket
- Two OpenVPX 1000Base-X Control Plane interfaces to VPX P1
- 2 Serial COM port interfaces to VPX P1
- Voltage and temperature monitoring
- Air-cooled and conduction-cooled configurations

1.2 References & Specifications

ANSI/VITA 46.0	*VPX Baseline Standard*, October 2007, VITA, ISBN 1-885731-44-2
ANSI/VITA 46.4	*PCI Express® on the VPX Fabric Connector*, July 2010, VITA, Draft 0.15
ANSI/VITA 46.6	*Gigabit Ethernet Control Plane on VPX*, September 2010, VITA, Draft 0.7
ANSI/VITA 46.9	*PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard*, November 2010, VITA, ISBN 1-885731-63-9
ANSI/VITA 48.2	*Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to VITA VPX*, July 2010, VITA, ISBN 1-885731-60-4
ANSI/VITA 57.1	*FPGA Mezzanine Card (FMC) Standard*, July 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 65	*OpenVPX™ System Specification*, June 2010, VITA, ISBN 1-885731-58-2
ANSI/VITA 57.4	*FPGA Mezzanine Card Plus(FMC+) Standard*, March 2016, VITA, Draft

Table 1 : References (continued on next page)

ANSI/VITA 66.0	*Optical Interconnect on VPX - Base Standard*, July 2016, VITA, ISBN 1-885731-90-6
ANSI/VITA 66.4	*Optical Interconnect On VPX – Half Width MT Variant*, April 2016, VITA, ISBN 1-885731-88-4

Table 1 : References

1.3 Order Code

ADM-VPX3-9Z2/z-2(c)(o)

Name	Symbol	Configurations
Zynq Ultrascale+™ device	z	15EG = ZU15EG , 9EG = ZU9EG (Contact factory for details)
Cooling	c	blank = air cooled commercial /AC1 = air cooled industrial /CC1 = conduction cooled industrial
Optics	o	blank= No optics fitted , /O = V66.4 Optics fitted

Table 2 : Build Options

Not all combinations are available. Please check with Alpha Data sales for details.

2 Installation

2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2 Hardware Installation

2.2.1 System Requirements

The ADM-VPX3-9Z2 is a 3U OpenVPX compliant FPGA card with FMC front IO interface.

Alpha Data offers a Rear Transition Module (RTM) that breaks out all P2 IO and P1 control lanes (Part number: ADM-VPX3-9Z2-RTM).

2.2.2 Cooling Requirements

The power dissipation of the board is highly dependent on the FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the approximate current requirements for each power rail.

The board is supplied with a passive air cooled or conduction cooled heatsink according to the order number given at time of purchase. It is the users responsibility to ensure sufficient airflow for air cooled applications and appropriate metalwork for conduction cooled applications.

The board features system monitoring that measures the board and FPGA temperature. It also includes a self-protection mechanism that will clear the target FPGA configuration if an over-temperature condition is detected.

See Section System Monitoring for health monitoring details.

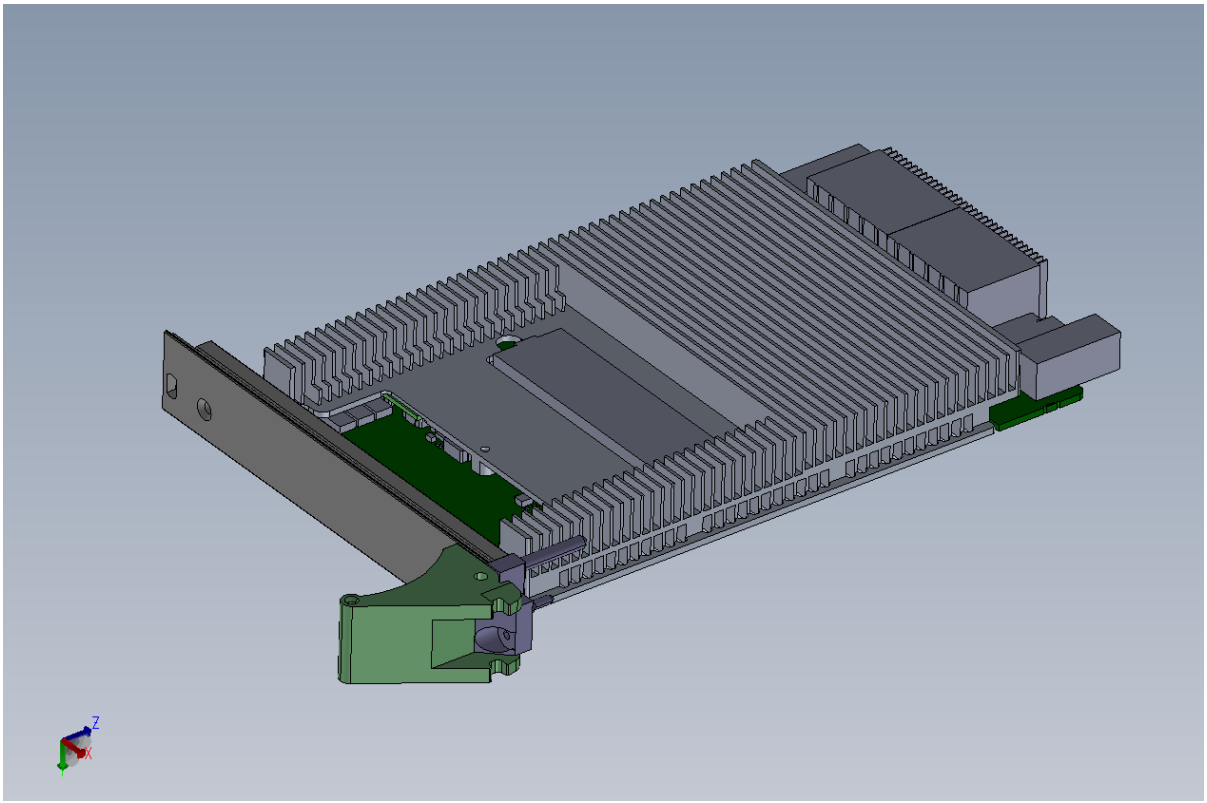

Figure 1 : ADM-VPX3-9Z2 Air Cooled

2.3 Software Installation

Please refer to the Reference Designs on the Alpha Data Download Site. Example projects for configuring the Zynq Ultrascale+ MPSOC device and example software for running on the ARM CPUs can be downloaded from there.

3 Functional Description

3.1 Overview

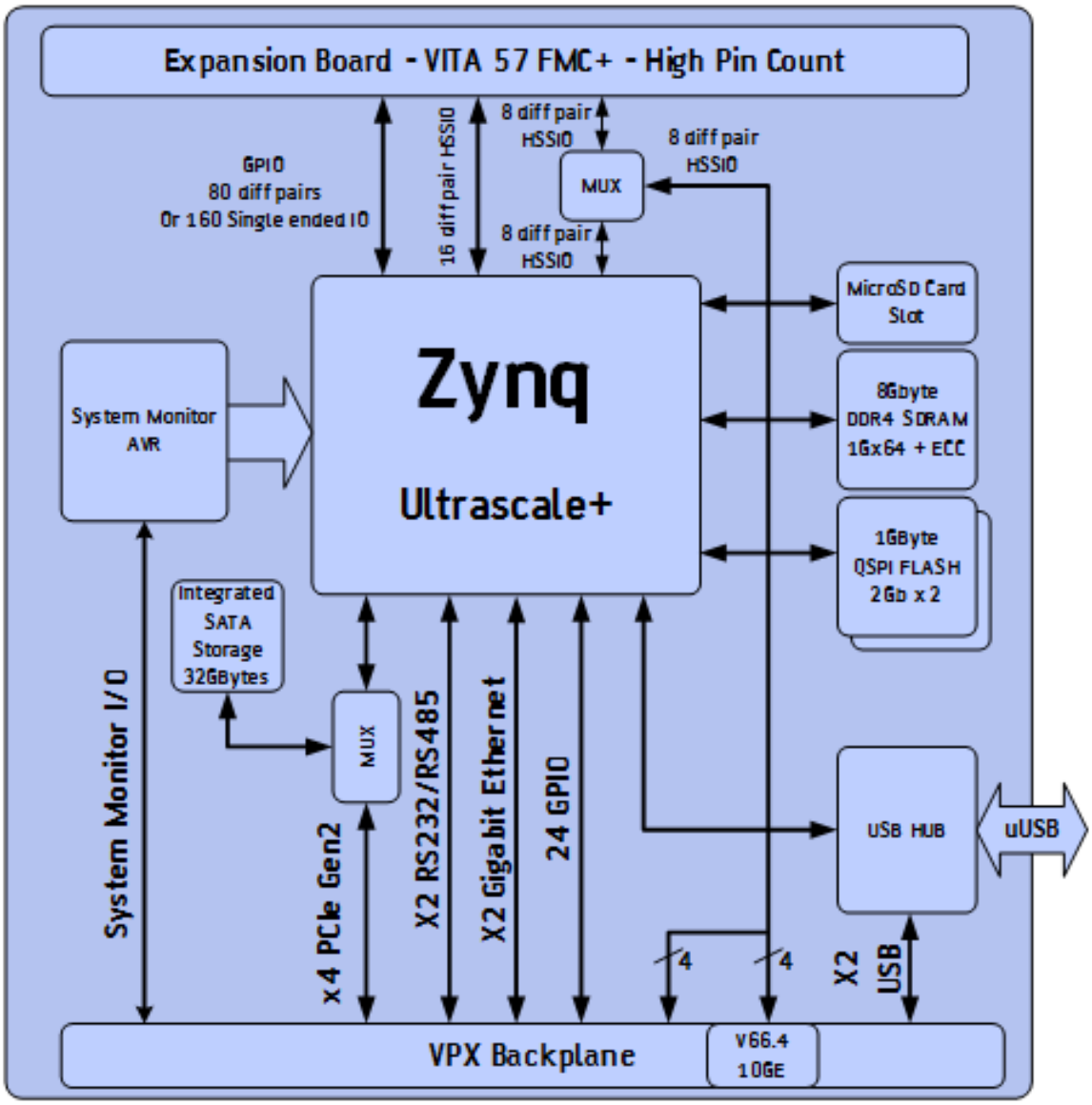

Figure 2 : ADM-VPX3-9Z2 Block Diagram

3.1.1 Switch Definitions

There are two push-button reset switches on the board. Their functions are detailed below.

Switch Ref.	Function	ON State	Off State
SW1	Hardware Reset	Hardware Reset (complete restart)	Normal Operation
SW2	Software Reset	Software Reset (warm reset)	Normal Operation

Table 3 : Reset Switch Definitions

There are two sets of eight DIP switches placed on the bottom of the board. Their functions are described below.

Note:
All switches are OFF by default. Factory Configuration switch must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
SW3-1	Spare (to FPGA pin AM14)	User defined	User defined
SW3-2	Internal Oscillator	Use VPX REFCLK	Use Internal Oscillator source
SW3-3	Internal SATA SSD Enable	Internal SSD is connected to PS HSSIO lane 1	PCIe lane (1) is connected to PS HSSIO lane 1
SW3-4	Flash Boot Inhibit	Target FPGA is not configured from onboard flash memory.	Target FPGA is configured from on-board flash memory.
SW3-5	VPX JTAG	Connect JTAG chain to P0	Isolate JTAG chain from P0
SW3-6	HSSIO_MUX_-SELECT A	FPGA MGT Bank 129 routed to FMC+ Socket	FPGA MGT Bank 129 connected to V66.4 Fibre
SW3-7	Factory Configuration	-	Normal Operation
SW3-8	HSSIO_MUX_-SELECT B	FPGA MGT Bank 130 routed to FMC+ Socket	FPGA MGT Bank 130 connected to VPX P1

Table 4 : VPX Control Switch Definitions (SW3)

Switch Ref.	Function	ON State	Off State
SW4-(4:1)	PS_MODE(3:0)	PS Boot Mode - see section Boot Modes	
SW4-5	PS_MUX_SEL0	PS HSSIO lane 0 connected to PCIe (0)	PS HSSIO lane 0 connected to VPX P1
SW4-6	PS_MUX_SEL1	PS HSSIO lanes (2:1) connected to PCIe(2:1)	PS HSSIO lanes (2:1) connected to VPX P1
SW4-7	nSD_EMMC	SD Card enabled	eMMC device enabled
SW4-8	SD_WP	SD Card Write Protected (must be enabled in software)	SD Card Write Enabled

Table 5 : Processor Setup Switch Definitions (SW4)

3.1.2 LED Definitions

There are seven LEDs to provide a visual indication of the board status.

Their locations are shown in Figure 3

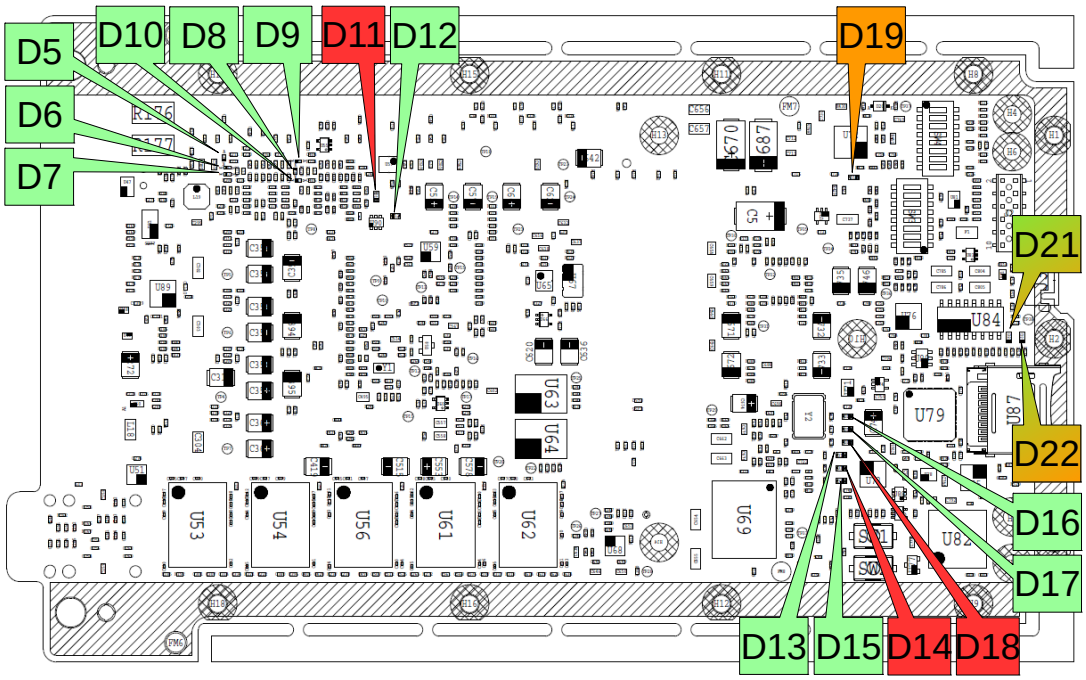

Figure 3 : LED Locations

Comp. Ref.	Function	ON State	Off State
D13 (Green)	System Monitor Status	See Table 26	
D18 (Red)	System Monitor Status	See Table 26	
D15 (Green)	FPGA (PL) Done	PL is configured	PL is not configured
D19 (Amber)	VPX JTAG STATUS	JTAG chain Connected to VPX P0	JTAG chain isolated from VPX P0
D14 (Red)	Power Fault	Power Supply Fault	Power Supplies off or within range
D11 (Red)	PS Error	PS Error	Normal Operation
D12 (Green)	PS Status	Normal Operation	PS is in Reset / Error
D16 (Green)	SATA PHY	Link Established	No Link
D17 (Green)	SATA DAS	Data transfer in progress	Disk Idle

Table 6 : Main LED Definitions

A further two sets of three LEDs provide an indication of the status of the two Ethernet interfaces

Comp. Ref.	Function	ON State	Off State
D9 (Green)	Ethernet 0 LED0	See Table 19	
D8 (Green)	Ethernet 0 LED1	See Table 19	
D10 (Green)	Ethernet 0 LED2	See Table 19	
D5 (Green)	Ethernet 1 LED0	See Table 19	
D6 (Green)	Ethernet 1 LED1	See Table 19	
D7 (Green)	Ethernet 1 LED2	See Table 19	

Table 7 : Ethernet LED Definitions

Two Bi-Colour LEDs provide an indication of the status of the two USB interfaces

Comp. Ref.	Function	ON State	Off State
D22 (Bi-Green)	USB1 Status	Normal Operation	Not Operational
D22 (Bi-Amber)	USB1 Error	Error	Normal Operation
D21 (Bi-Green)	USB2 Status	Normal Operation	Not Operational
D21 (Bi-Amber)	USB2 Error	Error	Normal Operation

Table 8 : USB LED Definitions

3.2 VPX P0 Interface

3.2.1 SYSRESET#

VPX Reset In. This signal is an active low input from the system. When asserted, the PS PCIe interface will be reset.

The SYSRESET# signal is translated to 1.8V levels and connected to the FPGA at MIO pin J22.

3.2.2 AUXCLK

Auxiliary Clock. This clock is a direct input to the target FPGA. In OpenVPX this clock line is used for 1PPS synchronization signaling. The prefered signaling standard is LVDS.

AUXCLK_P is connected to FPGA GC pin E22

AUXCLK_N is connected to FPGA GC pin D22

3.2.3 REFCLK

Reference Clock. This clock is an input to the onboard clock distribution and generation system. The 50MHz defined in OpenVPX can be used to align all system clocks. Alternatively an onboard 25MHz reference can be generated as shown in VPX Control Switch Definitions (SW3).

3.3 VPX P2 GPIO

3.3.1 LVDS

The GPIO on P2 is compatible with 2.5V signaling such as LVDS and 2.5V single ended signals.

These signals are routed differentially. The FPGA is protected from inappropriate signal levels by a low resistance quick switch that clamps at 2.5V in either direction, but can accept up to 3.3V on an input.

3.4 JTAG Interface

3.4.1 On-board Interface

A JTAG boundary scan chain is connected to header J2. This allows the connection of the Xilinx JTAG cable.

The scan chain is shown in Figure JTAG Boundary Scan Chain:

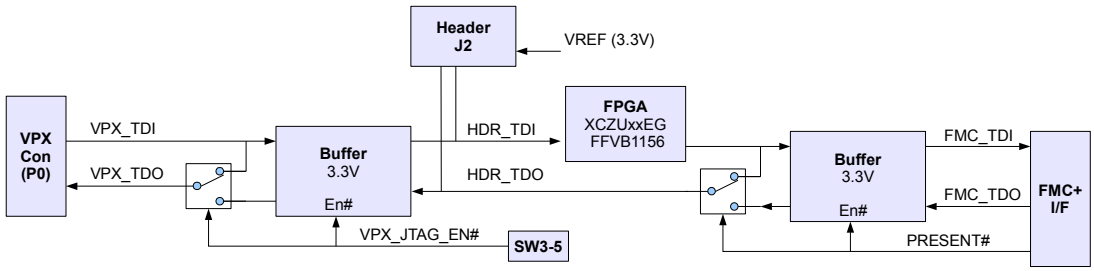

Figure 4 : JTAG Boundary Scan Chain

If the boundary scan chain is connected to the interface at the VPX backplane (SW3-5 is ON), header J2 should not be used.

3.4.2 VPX Interface

The JTAG interface on the VPX backplane is normally unused. When SW3-5 is OFF (default), all JTAG signals to P0 are left floating.

The JTAG interface can be connected to the VPX Backplane (through level-translators) by switching SW3-5 ON.

3.4.3 JTAG Voltages

The on-board JTAG scan chain uses 3.3V. The Vcc supply provided on J2 to the JTAG cable is +3.3V and is protected by a poly fuse rated at 350mA.

The JTAG signals at the VPX interface use 3.3V signal levels and are connected through buffers to the on-board scan chain.

The JTAG signals at the FMC interface also use 3.3V signal levels and are connected through buffers to FMC boards scan chain.

3.5 Clocks

The **ADM-VPX3-9Z2** board provides a wide variety of clocking options. In addition to the clocks routed from the FMC+ connector, the board has 2 user-programmable clock generators. These clocks can be combined with the FPGA's internal PLLs to suit a wide variety of communication protocols.

A complete overview of the clock routing on the **ADM-VPX3-9Z2** is given in Clocks. A description of each clock follows.

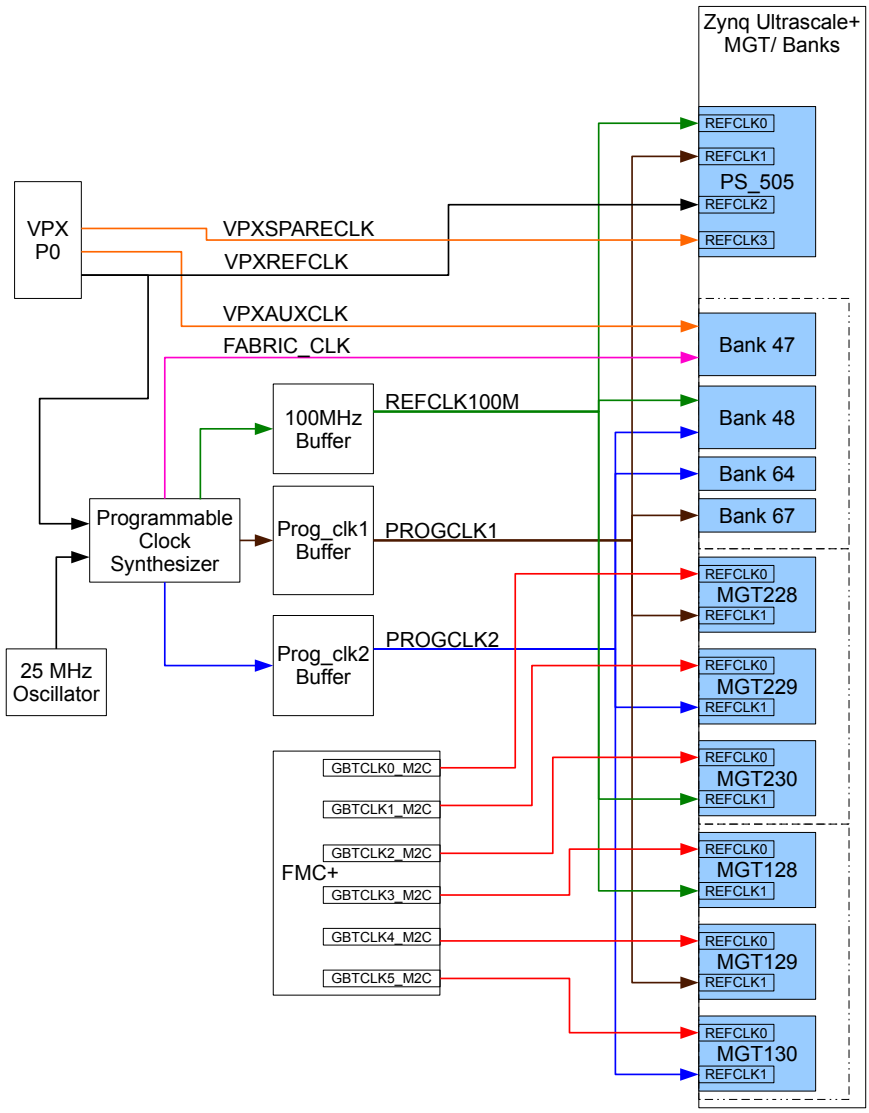

Figure 5 : Clocks

3.5.1 IO Delay Reference Clock (FABRIC_CLK)

The fixed reference clock FABRIC_CLK is a differential LVDS signal.

FABRIC_CLK is used as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
FABRIC_CLK	300 MHz	IO BANK 47	LVDS	G21	F21

Table 9 : DDR REFCLK Connections

3.5.2 Fixed 100MHz Reference clock REFCLK100M

A fixed 100MHz reference clock is available on the board.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin
REFCLK100M[0]	100 MHz	PS_505_MGTREFCLK_0	LVDS	AA27
REFCLK100M[1]	100 MHz	IO BANK 48	LVDS	E17
REFCLK100M[2]	100 MHz	MGTREFCLK1_230	LVDS	B10
REFCLK100M[3]	100 MHz	MGTREFCLK1_128	LVDS	N27

Table 10 : REFCLK100M Connections

3.5.3 Programmable Clocks (PROGCLK1 and PROGCLK2)

There are two programable clock sources that are forwarded throughout the FPGA. These clocks can be programmed via the avr2util utility contained within the Alpha Data ADM-VPX3-9Z2 SDK. PROGCLK1 and PROGCLK2 are generated by a dedicated programmable clock generator IC and offer extremely high frequency resolutions (1ppm increments).

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
PROGCLK1[0]	5 - 400 MHz	PS_505_MGTREFCLK_1	LVDS	W27	W28
PROGCLK1[1]	5 - 400 MHz	IO BANK 67	LVDS	R10	R9
PROGCLK1[2]	5 - 400 MHz	MGTREFCLK1_228	LVDS	J8	J7
PROGCLK1[3]	5 - 400 MHz	MGTREFCLK1_129	LVDS	J27	J28

Table 11 : PROGCLK1 Connections

Note: PROGCLK1[3:0] are all buffered copies of the same clock signal.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
PROGCLK2[0]	5 - 400 MHz	IO BANK 48	LVDS	E19	D19
PROGCLK2[1]	5 - 400 MHz	IO BANK 64	LVDS	AK8	AK7
PROGCLK2[2]	5 - 400 MHz	MGTREFCLK1_130	LVDS	E27	E28
PROGCLK2[3]	5 - 400 MHz	MGTREFCLK1_229	LVDS	E8	E7

Table 12 : PROGCLK2 Connections

Note: PROGCLK2[3:0] are all buffered copies of the same clock signal.

3.5.4 Module to Carrier Global Clocks (CLK_M2C)

A connected FMC+ board can generate a number of differential Global clocks (as per the FMC standard). They each connect to an global clock input on the FPGA.

Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
CLK_M2C_0	Variable	Bank 66	LVDS	Y5	AA5
CLK_M2C_1	Variable	Bank 66	LVDS	Y4	Y3
CLK_M2C_2	Variable	Bank 65	LVDS	AF6	AG6
CLK_M2C_3	Variable	Bank 65	LVDS	AE7	AF7

Table 13 : CLK_M2C Connections

3.5.5 Module to Carrier MGTREF Clocks (GBTCLK_M2C)

A connected FMC board can generate a number of differential MGT Reference clocks (as per the FMC standard) . They each connect to an MGTREFCLK input on the FPGA.

Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
GBTCLK_0_M2C	Variable	MGTREFCLK_228	LVDS	L8	L7
GBTCLK_1_M2C	Variable	MGTREFCLK_229	LVDS	G8	G7
GBTCLK_2_M2C	Variable	MGTREFCLK_230	LVDS	C8	C7
GBTCLK_3_M2C	Variable	MGTREFCLK_128	LVDS	R27	R28
GBTCLK_4_M2C	Variable	MGTREFCLK_129	LVDS	L27	L28
GBTCLK_5_M2C	Variable	MGTREFCLK_130	LVDS	G27	G28

Table 14 : GCLK_M2C Connections

3.5.6 PS_REFCLK

The PS reference clock is an independent 50.0MHz reference clock. This is the master clock of the PS side of the MPSoC.

Signal	Frequency	FPGA Input	IO Standard	pin
PS_REFCLK	50MHz	PS_REF_CLK (Bank 503)	LVCMOS18	U24

Table 15 : PS_REFCLK Connection

3.5.7 VIDEO_CLK

An optional independent 27.0MHz reference clock is provided. This can be used to clock the video sections in the PS side of the MPSoC.

Signal	Frequency	FPGA Input	IO Standard	pin
VIDEO_REFCLK	27MHz	PS_MIO27 (Bank 501)	LVCMOS18	M21

Table 16 : VIDEO_REFCLK Connection

3.5.8 USB_REFCLK24M

The USB PHY and hub are provided with an independent 24.0MHz reference clock. This clock is asynchronous to the clocks generated by the Si5338B and is not connected to the Zynq SoC.

3.5.9 ETH_CLK25M

The Ethernet PHYs are provided with an independant 25.0MHz reference clock. This clock is asynchronous to the clocks generated by the Si5338B and is not connected to the Zynq SoC..

3.6 Resets

The Zynq PS can be reset via the two push button switches, SW1 and SW2.

Switch	Reset Type	Effect
SW1	Power on Reset (PS_POR_B pin)	Clears all logic. Mode pins sampled (i.e. reconfigures hardware). Reboots MPSoC.
SW2	Soft Reset (PS_SRST_B pin)	Same as Power on Reset - but does not sample Mode pins (hardware configuration unchanged).

Table 17 : Reset Switches

3.7 Zynq PS Block

3.7.1 Boot Modes

PS_MODE3 (SW4-4)	PS_MODE2 (SW4-3)	PS_MODE1 (SW4-2)	PS_MODE0 (SW4-1)	Boot Mode
ON	ON	ON	ON	JTAG
ON	ON	ON	OFF	Quad SPI (24 bit addressing)
ON	ON	OFF	ON	Quad SPI (32 bit addressing)
ON	ON	OFF	OFF	SD Flash - SD 2.0
ON	ON	ON	ON	eMMC v4.5 at 1.8V

Table 18 : Boot Mode Selection

Note: all other possible switch settings are reserved / invalid.

3.7.2 PS Memory Interfaces

The memory devices attached to the PS side of the MPSoC are outlined below.

3.7.2.1 Quad SPI Flash Memory

The ADM-VPX3-9Z2 has two Quad SPI Flash devices, up to 2Gb each. They can be interfaced seperately in x1, x2,x4 modes or together in x8 mode.

3.7.2.2 MicroSD and eMMC Flash Memories

The ADM-VPX3-9Z2 can interface to either a MicroSD card (SD 2.0 standard at 3.3V) or an eMMC device (v4.5 at 1.8V).

The Switch SW4-7 determines which of the two interfaces is in use (as they share common MIO pins).

The uSD card should be fitted in socket U87.

3.7.2.3 PS DDR4 Memory

The PS side of the MPSoC is connected to 1 bank of DDR4-2400 SDRAM, 1GB x72, 8GB total + ECC

3.7.3 Ethernet Interfaces

The **9Z2** has two SGMII Serial Ethernet Interfaces at VPX connector P1. Both Ethernet Interfaces are connected to the MPSoC PS.

Both interfaces have a Marvell 88E1512 PHY, connected to the PS via RGMII.

The Zynq PS MDIO interface is also connected to the VPX connector via buffers.

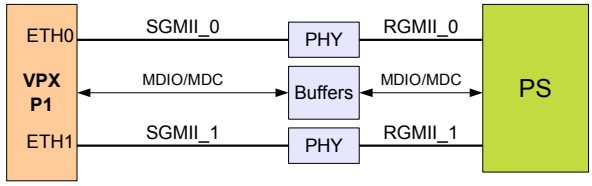

Figure 6 : Ethernet Interfaces

Each interface has three status LEDs. The functions of these are shown in Table 19below.

LED	Colour	Function
0	Green	On = 1000M link speed
1	Green	On or Flashing = Activity
2	Green	On = Link up

Table 19 : Ethernet Status LEDs

3.7.4 Serial COM Ports

There are two serial COM ports connected to VPX connector P1, as shown in Figure Serial COM Ports.

COM2 uses RS-232 by default but may be configured for RS-485 operation. Please contact Alpha Data for further details of the RS-485 mode.

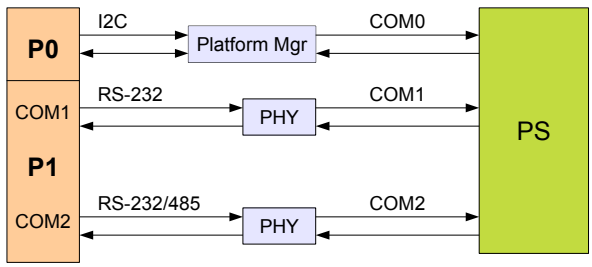

Figure 7 : Serial COM Ports

3.7.5 USB Interfaces

The **9Z2** has three external USB interfaces.

Interfaces USB1 and USB2 are connected between VPX P1 connector and the PS side of the MPSoC.

The PS acts as the USB host to interfaces USB1 and USB2.

USB3 is a direct connection between microUSB connector J3 and the Platform Manager / System Monitor Microcontroller.

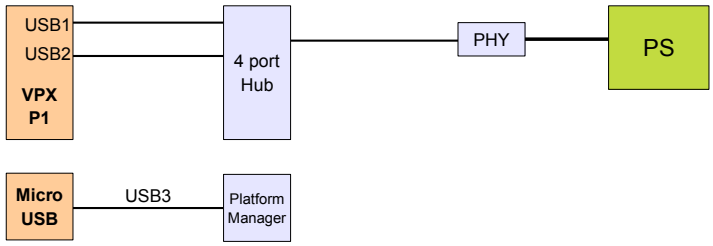

Figure 8 : USB Interfaces

3.8 Zynq PL Block

3.8.1 I/O Bank Voltages

The FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in PL FPGA IO Banks.

IO Banks	Voltage	Purpose
65, 66, 67	FMC_VADJ	FMC+ GPIO - LA and HA
64	FMC_VIO_B	FMC+ GPIO - HB
25, 46, 47	FMC3_VADJ	FMC+ GPIO
47, 48	2.5V	VPX P2 GPIO
50	3.3V	Optical Module Setup and Control
49	1.8V	Unused

Table 20 : PL FPGA IO Banks

3.8.2 PL MGT Links

There are a total of 32 Multi-Gigabit Transceiver (MGT) links connected to the FPGA:

Links	Banks	Width	Max Rate	Connection
DP(15:0)	228, 229, 230, 128	16	24Gbps	Direct links to FMC+ Socket (J1)
DP(19:16)	129	4	12Gbps	Links muxed to EITHER FMC+ Socket (J1) OR VPX P2 Optical Module
DP(23:20)	130	4	12Gbps	Links muxed to EITHER FMC+ Socket (J1) OR VPX P1 Connector

Table 21 : PL MGT Links

Note: Links that are multiplexed are restricted to a maximum bitrate of 12Gbps.

3.8.3 FMC+ GPIO Interface

The FMC+ Connector (J1) has GPIO connections arranged as follows:

Group	FPGA Bank	Name	Function
LA_0	66	LA(12:2)	11 diff. Pairs / 22 single-ended
		LA_CC (1:0)	2x Regional Clocks / GPIO pairs / 4 single-ended
LA_1	65	LA(33:19)	15 diff. Pairs / 30 single-ended
		LA_CC (18:17)	2x Regional Clocks / GPIO pairs / 4 single-ended
HA_0	66,67	HA(16:2)	15 diff. Pairs / 30 single-ended
		HA_CC (1:0)	2x Regional Clocks / GPIO pairs / 4 single-ended
		HA(23:18)	6 diff. Pairs / 12 single-ended
		HA_CC (17)	Regional Clock / GPIO pair / 2 single-ended
HB_0	64	HB(5:1)	5 diff. Pairs / 10 single-ended
		HB(16:7)	10 diff. Pairs / 20 single-ended
		HB(21:18)	4 diff. Pairs / 8 single-ended
		HB_CC (0)	Regional Clock / GPIO pair / 2 single-ended
		HB_CC (6)	Regional Clock / GPIO pair / 2 single-ended
		HB_CC (17)	Regional Clock / GPIO pair / 2 single-ended

Table 22 : FMC+ Groups (J1)

3.8.4 VPX P2 GPIO Interface

The P2 VPX Connector has GPIO connections arranged as follows:

Group	FPGA Bank	Name	Function
GPIO_0	48	GP(8:1)	8 diff. Pairs / 16 single-ended
GPIO_1	47	GP(12:9)	4 diff. Pairs / 8 single-ended

Table 23 : VPX P2 GPIO Groups

3.9 System Monitoring

The **9Z2** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using an Atmel AVR microcontroller (uC).

The microcontroller continually measures all voltage rails and temperature sensors and transmits the results to the FPGA, where they are stored in blockram.

The following voltage rails and temperatures are monitored by the microcontroller:

Monitor	*Purpose*
12V0	12V Board Input Supply
5V0	5V Board Input Supply
3V3	Board Input Supply
2V5	FPGA IO Supply
1V8	FPGA IO Supply
0V85	FPGA Core Voltage
MGT_AUX_1V8	FPGA MGT Aux Supply
1V2	DDR4 SDRAM, Target FPGA memory I/O
FMC_VADJ	Variable FMC IO Supply
0V85_BRAM	FPGA Block RAM Voltage
MGT_1V2	FPGA MGT Vtt Supply
MGT_0V9	FPGA MGT Vcc Supply
PSINTFP_0V85	MPSoC PS Core Supply
Temp1	microcontroller internal temperature
Temp2	TMP422 internal temperature
Temp3	FPGA on-die temperature (measured in TMP422)

Table 24 : Voltage and Temperature Monitors (in microcontroller)

The system monitor sensor values can be read via usb using the avr2util utility contained within the Alpha Data ADM-VPX3-9Z2 SDK.

3.9.1 Automatic Temperature Monitoring

The system monitor checks that the board and FPGA are being operated within the specified limits. If the temperature is close to the limit, a "Warning Alarm" interrupt is set.

If a limit is exceeded, a "Critical Alarm" interrupt is set. After the Critical Alarm is set, there is a 5 second delay before the system monitor unconfigures the FPGA by asserting its "PROG" pin.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

The temperature limits are shown in Table Temperature Limits. Note that the Min and Max values include a 5°C margin to prevent measurement errors triggering a false alarm.

	Target FPGA				Board (uC and PCB)			
	Min	Lower Warning	Upper Warning	Max	Min	Lower Warning	Upper Warning	Max
Extended	-5°C	+5°C	+95°C	+105°C	-5°C	+5°C	+80°C	+90°C
Industrial	-45°C	-35°C	+95°C	+105°C	-45°C	-35°C	+80°C	+90°C

Table 25 : Temperature Limits

3.9.2 System Monitor Status LEDs

LEDs D13 (Green) and D18 (Red) indicate the microcontroller status.

LEDs	*Status*
Flashing Green + Flashing Red (alternate)	Service Mode
Red	Missing application firmware or invalid firmware
Red + Green	Standby (Powered off)
Green	Running and no alarms
Flashing Green + Red	Attention - alarm active
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Red	FPGA configuration cleared to protect board

Table 26 : System Monitor Status LEDs

3.10 FMC Interface and Front-Panel I/O

The FMC+ interface provides a high-performance and flexible front-panel interface through a range of interchangeable, industry standard IO modules which connect at receptacle J1.

The FMC+ interface adheres to VITA 57.4. The ADM-VPX3-9Z2 utilizes all possible FMC+ connectivity. This includes all GPIO, all MGT links, and all clock capable IO.

FMC I2C signal (SCL and SDA at C30 and C31) are connected to the system monitor microcontroller. They are used to determine operating voltage during startup and are not accesable to the user.

The FMC Present signal (PRSNT_M2C_L at connector pin H2) is connected to the system monitor microcontroller.

Note:
The ADM-VPX3-9Z2 supports only 1.8V and lower VADJ Voltages.

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Appendix A: P1 Pin Assignments

Appendix A.1: Data Plane (P1 Wafers 1-4)

Signal	VPX P1	FPGA		FPGA	VPX P1	Signal
PCIE_TX0_P	D1	AB29	|	AB33	A1	PCIE_RX0_P
PCIE_TX0_N	E1	AB30	|	AB34	B1	PCIE_RX0_N
PCIE_TX1_P	E2	Y29	|	AA31	B2	PCIE_RX1_P
PCIE_TX1_N	F2	Y30	|	AA32	C2	PCIE_RX1_N
PCIE_TX2_P	D3	W31	|	Y33	A3	PCIE_RX2_P
PCIE_TX2_N	E3	W32	|	Y34	B3	PCIE_RX2_N
PCIE_TX3_P	E4	V29	|	V33	B4	PCIE_RX3_P
PCIE_TX3_N	F4	V30	|	V34	C4	PCIE_RX3_N

Table 27 : Data Plane (P1 Wafers 1-4)

Appendix A.2: Data/Expansion Plane (P1 Wafers 5-8)

Signal	VPX P1	FPGA		FPGA	VPX P1	Signal
P1_MUX_TX_P_0	E6	F29	|	B6	A13	P1_MUX_RX_P_0
P1_MUX_TX_N_0	F6	F30	|	C6	B13	P1_MUX_RX_N_0
P1_MUX_TX_P_1	D7	D29	|	A7	B14	P1_MUX_RX_P_1
P1_MUX_TX_N_1	E7	D30	|	B7	C14	P1_MUX_RX_N_1

Table 28 : Data/Expansion Plane (P1 Wafers 5-8)

Appendix A.3: Expansion/User Plane (P1 Wafers 9-14)

Signal	VPX P1	FPGA		FPGA	VPX P1	Signal
P1_TX1_P	E10	AB29	|	AB33	B10	P1_RX1_P
P1_TX1_N	F10	AB30	|	AB34	C10	P1_RX1_N
P1_TX2_P	D11	W31	|	Y33	A11	P1_RX2_P
P1_TX2_N	E11	W32	|	Y34	B11	P1_RX2_N
P1_TX3_P	E12	V29	|	V33	B12	P1_RX3_P
P1_TX3_N	F12	V30	|	V34	C12	P1_RX3_N
P1_MUX_TX_P_2	D13	B29	|	C31	A13	P1_MUX_RX_P_2
P1_MUX_TX_N_2	E13	B30	|	C32	B13	P1_MUX_RX_N_2
P1_MUX_TX_P_3	E14	A31	|	B33	B14	P1_MUX_RX_P_3
P1_MUX_TX_N_3	F14	A32	|	B34	C14	P1_MUX_RX_N_3

Table 29 : Expansion/User Plane (P1 Wafers 9-14)

Appendix A.4: Control Plane (P1 Wafers 15-16)

Signal	VPX P1	Component.Pin		Component.Pin	VPX P1	Signal
ETH2_TX_P	D15	U35.4	|	U35.1	A15	ETH2_RX_P
ETH2_TX_N	E15	U35.5	|	U35.2	B15	ETH2_RX_N
ETH1_TX_P	E16	U32.4	|	U32.1	B16	ETH1_RX_P
ETH1_TX_N	F16	U32.5	|	U32.2	C16	ETH1_RX_N

Table 30 : Control Plane (P1 Wafers 15-16)

Appendix B: P2 Pin Assignments

Appendix B.1: GPIO (P2 Wafers 4-6)

Signal	VPX P2	FPGA		FPGA	VPX P2	Signal
GP1_N	F6	H17	|	C19	E3	GP7_N
GP1_P	E6	J17	|	C18	D3	GP7_P
GP2_N	C6	K17	|	B19	B3	GP8_N
GP2_P	B6	L17	|	B18	A3	GP8_P
GP3_N	E5	K18	|	C22	F2	GP9_N
GP3_P	D5	L18	|	D21	E2	GP9_P
GP4_N	B5	H19	|	B21	C2	GP10_N
GP4_P	A5	H18	|	C21	B2	GP10_P
GP5_N	F4	C17	|	A22	E1	GP11_N
GP5_P	E4	D17	|	A21	D1	GP11_P
GP6_N	C4	A18	|	A20	B1	GP12_N
GP6_P	B4	A17	|	B20	A1	GP12_P

Table 31 : GPIO (P2 Wafers 4-6)

Appendix C: FMC Pin Assignments

Appendix C.1: GPIO Pins

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
LA00_CC_N	G7	AA6	|	N11	F5	HA00_CC_N
LA00_CC_P	G6	AA7	|	P11	F4	HA00_CC_P
LA01_CC_N	D9	Y7	|	R8	E3	HA01_CC_N
LA01_CC_P	D8	Y8	|	T8	E2	HA01_CC_P
LA02_N	H8	AC6	|	M14	K8	HA02_N
LA02_P	H7	AC7	|	M15	K7	HA02_P
LA03_N	G10	AC4	|	N12	J7	HA03_N
LA03_P	G9	AB4	|	P12	J6	HA03_P
LA04_N	H11	AC8	|	K15	F8	HA04_N
LA04_P	H10	AB8	|	L15	F7	HA04_P
LA05_N	D12	W4	|	K16	E7	HA05_N
LA05_P	D11	W5	|	L16	E6	HA05_P
LA06_N	C11	W6	|	N8	K11	HA06_N
LA06_P	C10	W7	|	N9	K10	HA06_P
LA07_N	H14	U4	|	K12	J10	HA07_N
LA07_P	H13	U5	|	L12	J9	HA07_P
LA08_N	G13	AB5	|	L11	F11	HA08_N
LA08_P	G12	AB6	|	M11	F10	HA08_P
LA09_N	D15	V3	|	K13	E10	HA09_N
LA09_P	D14	V4	|	L13	E9	HA09_P
LA10_N	C15	V1	|	R13	K14	HA10_N
LA10_P	C14	V2	|	T13	K13	HA10_P
LA11_N	H17	Y1	|	R12	J13	HA11_N
LA11_P	H16	Y2	|	T12	J12	HA11_P
LA12_N	G16	W1	|	M13	F14	HA12_N
LA12_P	G15	W2	|	N13	F13	HA12_P
LA13_N	D18	AA1	|	L10	E13	HA13_N
LA13_P	D17	AA2	|	M10	E12	HA13_P
LA14_N	C19	AC3	|	V11	J16	HA14_N
LA14_P	C18	AB3	|	V12	J15	HA14_P
LA15_N	H20	AC1	|	U6	F17	HA15_N

Table 32 : GPIO Pins (continued on next page)

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
LA15_P	H19	AC2	|	V6	F16	HA15_P
LA16_N	G19	AA10	|	T6	E16	HA16_N
LA16_P	G18	AA11	|	T7	E15	HA16_P
LA17_CC_N	D21	AF5	|	P9	K17	HA17_CC_N
LA17_CC_P	D20	AE5	|	P10	K16	HA17_CC_P
LA18_CC_N	C23	AG4	|	T10	J19	HA18_N
LA18_CC_P	C22	AG5	|	U10	J18	HA18_P
LA19_N	H23	AE9	|	V7	F20	HA19_N
LA19_P	H22	AD10	|	V8	F19	HA19_P
LA20_N	G22	AF12	|	U8	E19	HA20_N
LA20_P	G21	AE12	|	U9	E18	HA20_P
LA21_N	H26	AH3	|	AC9	K20	HA21_N
LA21_P	H25	AG3	|	AB9	K19	HA21_P
LA22_N	G25	AG11	|	AA12	J22	HA22_N
LA22_P	G24	AF11	|	Y12	J21	HA22_P
LA23_N	D24	AH11	|	Y9	K23	HA23_N
LA23_P	D23	AH12	|	Y10	K22	HA23_P
LA24_N	H29	AJ2	|	AL7	K26	HB00_CC_N
LA24_P	H28	AH2	|	AL8	K25	HB00_CC_P
LA25_N	G28	AJ1	|	AM11	J25	HB01_N
LA25_P	G27	AH1	|	AL11	J24	HB01_P
LA26_N	D27	AF1	|	AK10	F23	HB02_N
LA26_P	D26	AF2	|	AJ10	F22	HB02_P
LA27_N	C27	AF3	|	AM10	E22	HB03_N
LA27_P	C26	AE3	|	AL10	E21	HB03_P
LA28_N	H32	AJ5	|	AK9	F26	HB04_N
LA28_P	H31	AJ6	|	AJ9	F25	HB04_P
LA29_N	G31	AJ4	|	AM8	E25	HB05_N
LA29_P	G30	AH4	|	AM9	E24	HB05_P
LA30_N	H35	AH8	|	AL5	K29	HB06_CC_N
LA30_P	H34	AG8	|	AL6	K28	HB06_CC_P
LA31_N	G34	AH6	|	AP10	J28	HB07_N
LA31_P	G33	AH7	|	AP11	J27	HB07_P
LA32_N	H38	AG9	|	AK4	F29	HB08_N
LA32_P	H37	AG10	|	AK5	F28	HB08_P
LA33_N	G37	AF8	|	AP4	E28	HB09_N

Table 32 : GPIO Pins (continued on next page)

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
LA33_P	G36	AE8	|	AP5	E27	HB09_P
HB16_N	F35	AP2	|	AN1	K32	HB10_N
HB16_P	F34	AN2	|	AM1	K31	HB10_P
HB17_CC_N	K38	AM5	|	AL2	J31	HB11_N
HB17_CC_P	K37	AM6	|	AL3	J30	HB11_P
HB18_N	J37	AP9	|	AK2	F32	HB12_N
HB18_P	J36	AN9	|	AK3	F31	HB12_P
HB19_N	E34	AL1	|	AN4	E31	HB13_N
HB19_P	E33	AK1	|	AM4	E30	HB13_P
HB20_N	F38	AP6	|	AP8	K35	HB14_N
HB20_P	F37	AN6	|	AN8	K34	HB14_P
HB21_N	E37	AP3	|	AP7	J34	HB15_N
HB21_P	E36	AN3	|	AN7	J33	HB15_P
FMC_CLK_DIR	B1	V9	|	-	-	-

Table 32 : GPIO Pins

Appendix C.2: Clock Pins

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
CLK0_M2C_N	H5	AA5	|	AG6	K5	CLK2_BIDIR_N
CLK0_M2C_P	H4	Y5	|	AF6	K4	CLK2_BIDIR_P
CLK1_M2C_N	G3	Y3	|	AF7	J3	CLK3_BIDIR_N
CLK1_M2C_P	G2	Y4	|	AE7	J2	CLK3_BIDIR_P
GBTCLK0_M2C_N	D5	L7	|	R28	L9	GBTCLK3_M2C_N
GBTCLK0_M2C_P	D4	L8	|	R27	L8	GBTCLK3_M2C_P
GBTCLK1_M2C_N	B21	G7	|	L28	L5	GBTCLK4_M2C_N
GBTCLK1_M2C_P	B20	G8	|	L27	L4	GBTCLK4_M2C_P
GBTCLK2_M2C_N	L13	C7	|	G28	Z21	GBTCLK5_M2C_N
GBTCLK2_M2C_P	L12	C8	|	G27	Z20	GBTCLK5_M2C_P

Table 33 : Clock Pins

Appendix C.3: MGT Pins

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
DP0_M2C_N	C7	T1	|	R3	C3	DP0_C2M_N
DP0_M2C_P	C6	T2	|	R4	C2	DP0_C2M_P
DP1_M2C_N	A3	P1	|	P5	A23	DP1_C2M_N
DP1_M2C_P	A2	P2	|	P6	A22	DP1_C2M_P
DP2_M2C_N	A7	M1	|	N3	A27	DP2_C2M_N
DP2_M2C_P	A6	M2	|	N4	A26	DP2_C2M_P
DP3_M2C_N	A11	L3	|	M5	A31	DP3_C2M_N
DP3_M2C_P	A10	L4	|	M6	A30	DP3_C2M_P
DP4_M2C_N	A15	K1	|	K5	A35	DP4_C2M_N
DP4_M2C_P	A14	K2	|	K6	A34	DP4_C2M_P
DP5_M2C_N	A19	J3	|	H5	A39	DP5_C2M_N
DP5_M2C_P	A18	J4	|	H6	A38	DP5_C2M_P
DP6_M2C_N	B17	H1	|	G3	B37	DP6_C2M_N
DP6_M2C_P	B16	H2	|	G4	B36	DP6_C2M_P
DP7_M2C_N	B13	F1	|	F5	B33	DP7_C2M_N
DP7_M2C_P	B12	F2	|	F6	B32	DP7_C2M_P
DP8_M2C_N	B9	D1	|	E3	B29	DP8_C2M_N
DP8_M2C_P	B8	D2	|	E4	B28	DP8_C2M_P
DP9_M2C_N	B5	C3	|	D5	B25	DP9_C2M_N
DP9_M2C_P	B4	C4	|	D6	B24	DP9_C2M_P
DP10_M2C_N	Y11	B1	|	B5	Z25	DP10_C2M_N
DP10_M2C_P	Y10	B2	|	B6	Z24	DP10_C2M_P
DP11_M2C_N	Z13	A3	|	A7	Y27	DP11_C2M_N
DP11_M2C_P	Z12	A4	|	A8	Y26	DP11_C2M_P
DP12_M2C_N	Y15	T34	|	T30	Z29	DP12_C2M_N
DP12_M2C_P	Y14	T33	|	T29	Z28	DP12_C2M_P
DP13_M2C_N	Z17	P34	|	R32	Y31	DP13_C2M_N
DP13_M2C_P	Z16	P33	|	R31	Y30	DP13_C2M_P
DP14_M2C_N	Y19	N32	|	P30	M19	DP14_C2M_N
DP14_M2C_P	Y18	N31	|	P29	M18	DP14_C2M_P
DP15_M2C_N	Y23	M34	|	M30	M23	DP15_C2M_N
DP15_M2C_P	Y22	M33	|	M29	M22	DP15_C2M_P
DP16_M2C_N	Z33	L32	|	K30	M27	DP16_C2M_N
DP16_M2C_P	Y35	K34	|	J32	M31	DP16_C2M_P

Table 34 : MGT Pins (continued on next page)

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
DP17_M2C_N	Z37	H34	|	H30	M35	DP17_C2M_N
DP17_M2C_P	Y39	F34	|	G32	M39	DP17_C2M_P
DP18_M2C_N	M15	E32	|	F30	Z9	DP18_C2M_N
DP18_M2C_P	M11	D34	|	D30	Y7	DP18_C2M_P
DP19_M2C_N	M7	C32	|	B30	Z5	DP19_C2M_N
DP19_M2C_P	M3	B34	|	A32	Y3	DP19_C2M_P
DP20_M2C_N	Z32	L31	|	K29	M26	DP20_C2M_N
DP20_M2C_P	Y34	K33	|	J31	M30	DP20_C2M_P
DP21_M2C_N	Z36	H33	|	H29	M34	DP21_C2M_N
DP21_M2C_P	Y38	F33	|	G31	M38	DP21_C2M_P
DP22_M2C_N	M14	E31	|	F29	Z8	DP22_C2M_N
DP22_M2C_P	M10	D33	|	D29	Y6	DP22_C2M_P
DP23_M2C_N	M6	C31	|	B29	Z4	DP23_C2M_N
DP23_M2C_P	M2	B33	|	A31	Y2	DP23_C2M_P

Table 34 : MGT Pins

Revision History

Date	Revision	Nature of Change
21 Sep 2018	0.1	Initial Draft
02 Jan 2020	1.0	First Release
16 Jan 2020	1.1	Added pinout tables

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Address: Suite L4A, 160 Dundee Street, Edinburgh, EH11 1DQ, UK
Telephone: +44 131 558 2600
Fax: +44 131 558 2700
email: sales@alpha-data.com
website: http://www.alpha-data.com

Address: 611 Corporate Circle, Suite H Golden, CO 80401
Telephone: (303) 954 8768
Fax: (866) 820 9956 - toll free
email: sales@alpha-data.com
website: http://www.alpha-data.com