
**Summary**

The **ADM-XRC-5LX** is a high performance reconfigurable PMC based on the Xilinx™ Virtex-5LX range of Platform FPGAs. Features include high speed PCI-X interface, external memory, high density I/O, programmable clocks, temperature monitoring, battery backed encryption (by using an appropriate XRM) and flash boot facilities.

A comprehensive cross platform API with support for **Microsoft Windows™**, **Linux** and **VxWorks** provides access to the full functionality of these hardware features.

**Features**
**Target Devices:**

Xilinx Virtex-5 - LX110, LX155 (FF1153)

**Memory:**

**SDRAM** - Up to 2GByte in 4 independent banks of DDR-II SDRAM @ 333MHz

**FLASH** - 4MByte serial Flash (connected to user FPGA)

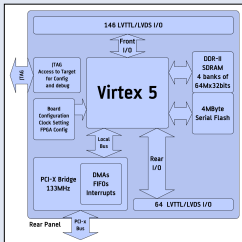
**FLASH** - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.

**Front Connector I/O:**

Up to 146 LVTTTL/LVDS I/O  
Programmable signaling levels of 1.8V, 2.5V or 3.3V

**Rear Connector I/O:**

64 I/O connections via PMC pn4 connector



Compatible Products					
XRM-ADC-02-125	Dual 14-bit ADC Interface (125Mbps)	XRM-ADC-03-1GG	Dual 8-bit ADC Interface (1.5Gbps)	XRM-ADC-06-250	Dual Channel ADC 250Mbps
XRM-ADC-54-3G	Single 8-bit ADC I/F (3Gbps)	XRM-CAMERALINK	Single Cameralink Interface	XRM-CLINK-MINI	Single/Dual Cameralink Interface
XRM-CLINK-ADV	Cameralink and JPEG2000	XRM-CLINK-GIGE	Cameralink and Gigabit Ethernet	XRM-DAC-03-275	Dual Channel 14-bit DAC
XRM-DAC-04-1G	Dual Channel 16-bit DAC	XRM-HD-SDI	Dual HDTV I/O Interface	XRM-0146	High Density Digital I/O
XRM-IC34	Digital I/O	XRM-VIDEO-I/O	Video I/O Interface	XRM-ZBT	ZBT Memory and RS232 Interfaces

**Specification**

Product Name	ADM-XRC-5LX
Target Devices	Xilinx Virtex-5 - LX110, LX155 (FF1153)
Host I/F	PCI/PCI-X
Interface	64-bit 66MHz PCI or 64-bit 133MHz PCI-X interface in separate bridge device with 64-bit 80MHz local bus 4 DMA controllers FIFO and interrupt controller.
Memory	<b>SDRAM</b> - Up to 2GByte in 4 independent banks of DDRII SDRAM @ 333MHz <b>FLASH</b> - 4MByte serial Flash (connected to user FPGA) <b>FLASH</b> - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.
Front I/O	Up to 146 LVTTTL/LVDS I/O Programmable signaling levels of 1.8V, 2.5V or 3.3V
Rear I/O	64 I/O connections via PMC pn4 connector
Clocks	Local bus programmable up to 100MHz Low-jitter user clock, programmable up to 640MHz Custom clock inputs available through XRM interface
Device Configuration	PCI Bus direct to SelectMAP port From Flash direct on power-up Via external JTAG connector
Software	Drivers for Microsoft Windows™, Linux and VxWorks API with template designs in VHDL and Verilog
Environmental	<b>Temperature:</b> Air cooled option Operating Temperature 0° to +55°C  <b>EMC:</b> FCC 47CFR Part 2 EN55022 Equipment Class B

**Ordering Codes**
**ADM-XRC-5LX(z-y(m))**

Virtex-5 Device	z	LX110
Virtex-5 Speed	y	1, 2, 3
Memory Size Fitted	m	BLANK= 1GByte, /2 = 2GByte

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