ADM-XRC-5T-DA1

PCI Mezzanine Card with High Speed ADC and DAC

User Guide

Version 1.0

Alpha Data
4 West Silvermills Lane
Edinburgh EH3 5BD
UK

Phone: +44 (0) 131 558 2600
Fax: +44 (0) 131 558 2700
Email: support@alphadata.co.uk

Alpha Data
2570 North First Street, Suite 440
San Jose, CA 95131
USA

Phone: (408) 467 5076
Fax: (866) 820 9956
Email: support@alpha-data.com

Table of Contents

Table of Tables

Table of Figures

1. Introduction

The ADM-XRC-5T-DA1 is a high performance PCI Mezzanine Card (PMC) aimed at applications requiring high-speed analogue sampling coupled with the signal processing capabilities of the Virtex-5 LX110T, LX155T, FX70T, FX100T or SX95T FPGAs from Xilinx.

Based on the proven technology of Alpha Data's ADM-XRC-5T1 architecture, it integrates a 12bit, 2.3 GHz DAC, an 8-bit 3GHz ADC and the core of the ADM-XRC-5T1 board on a PMC format board, together with connectors for clock inputs, trigger/auxiliary signal output and debug I/O. All connectors for the analogue section are MMCX sockets.

The card uses an FPGA PCI bridge developed by Alpha-Data supporting PCI-X and PCI. A high-speed, multiplexed, 32-bit address/data bus connects the bridge to the target (user) FPGA.

The card can also be fitted with a Primary XMC connector to provide high-speed serial links to the user FPGA.

1.1. Digital Specifications

The ADM-XRC-5T-DA1 supports high performance PCI-X / PCI operation without the need to integrate proprietary cores into the FPGA.

- Physically conformant to VITA 42 XMC Standard
- Physically conformant to IEEE P1386-2001 Common Mezzanine Card standard (with XMC connector removed)
- 8-lane PCIe / Serial RapidIO connections to User FPGA (via XMC connector)
- High performance PCI and DMA controllers
- Local bus speeds of up to 80 MHz
- Two independent banks of 64Mx32 DDRII SDRAM (512MB total)
- Two independent banks of 2Mx18 DDRII SSRAM (4Mx18 total)
- User clock programmable between 31.25MHz and 625MHz
- Stable low-jitter 200MHz clock for precision IO delays
- User rear panel PMC connector with 24 free IO signals
- Programmable I/O voltage on rear interface
- Supports 3.3V PCI or PCI-X at 64 bits

1.2. DAC Specifications

The DAC is a 12bit, 2.3 GHz device (Maxim MAX19692) which can operate in one of three modes to provide useable output in the first, second and third Nyquist zones. This permits direct digital synthesis of high-frequency and wideband signals in all three zones whilst maintaining excellent spurious and noise performance.

1.2.1. DAC Clock Input (J4)

Impedance : 50 Ohms, ac (transformer) coupled
Maximum Differential Input Level: 2.5 Vppk
Minimum Differential Input Level: 0.6 Vppk (0 dBm, fCLK ≤ 1.5GHz)
Minimum Differential Input Level: 2.0 Vppk (+10 dBm, fCLK = 2.3GHz)

Note that the minimum differential input level increases linearly between 1.5 GHz and 2.3 GHz so for intermediate frequencies, the minimum level can be calculated using the formula
0.6+1.75*(Fck-1.5), Fck in GHz.

1.2.2. DAC Output (J3)

Output: 50 Ohms, AC (transformer) coupled
Bandwidth: 5 MHz to 3000 MHz
Level: -4 dBm typical (400 mV ppk into 50 ohms)
SFDR : 60 dB typical 100 MHz to 600 MHz sine wave
50 dB typical 600 MHz to 850 MHz sine wave
SFDR measured using example code and clock running at 2.3 GHz.

1.3. ADC Specification

The ADC is an 8-bit, 3Gsamples/second device (National Semiconductor ADC08300) whose wide bandwidth (3GHz) permits operation in the first and second Nyquist zones.

1.3.1. ADC Clock Input (J6)

Impedance : 50 Ohms, ac (transformer) coupled
Nominal Differential Input Level: 1 Vppk (+4 dBm)
Minimum Differential Input Level: 0.6 Vppk (-4 dBm)
Maximum Differential Input Level: 2.0 Vppk (+10 dBm)

Note that the sampling frequency of the data is 2* the clock frequency; e.g. a clock frequency of 1.5 GHz generates a sample clock of 3 GHz.

Note: exceeding the maximum voltage limit may result in permanent degradation of converter performance.

1.3.2. ADC Input (J5)

Input: 50 Ohms (ac coupled)
Bandwidth (3 dB) : 5 MHz to 2000 MHz[1]
Full scale input : Programmable, +5.3 dBm to +10 dBm
(520 mV ppk to 880 mVppk at ADC input via 10 dB pad)
Accuracy: +/- 10 % of full scale setting.

Note: exceeding the maximum limit may result in permanent degradation of converter performance.

1.4. Auxiliary IO

Three connectors with FPGA IO capability are provided. One is intended for general purpose signalling/debug use whilst the other two (connected directly to the FPGA inputs so signalling levels must be limited to 2V5 LVTTL logic) are intended for use as a high-speed differential pair for ADC synchronisation, using the scheme outlined in National Semiconductor Application Bulletin AB0612. These connectors can also be used for single-ended signals by adjusting the termination configuration. Contact factory for details.

1.4.1. Aux (J9)

User configurable as input (default) or output
Input: 4k7 Ohms, dc coupled
Level: +3V3 LVTTL or +5V TTL (factory/user selectable via 0R links)

1.4.2. Differential Trigger (J7,J8)

Input: 100R differential (default)

---

[1] Bandwidth is limited by the composite response of the ADC bandwidth (-2 dB typical at 2 GHz) and the input transformer bandwidth (-1 dB typical at 2GHz). Typical loss at 3 GHz=-5 dB.

Level (differential): 100 mV ppk to 600 mV ppk
(common mode): 0.3V DC to 2.2VDC
Note: exceeding these limits may result in permanent damage to the FPGA.

2. Hardware Installation

This chapter explains how to install the ADM-XRC-5T-DA1 onto a PMC motherboard.

2.1. Motherboard requirements

The ADM-XRC-5T-DA1 is a 3.3V only PCI device and is not compatible with systems that use 5V signalling.

The ADM-XRC-5T-DA1 must be installed in a PMC motherboard that supplies +5.0V and +3.3V power to the PMC connectors. Ensure that the motherboard satisfies this requirement before powering it up.

2.2. Handling instructions

Observe SSD precautions when handling the cards to prevent damage to components by electrostatic discharge.

Avoid flexing the board.

2.3. Installing the ADM-XRC-5T-DA1 onto a PMC motherboard

Note: This operation should not be performed while the PMC motherboard is powered up.

The ADM-XRC-5T-DA1 must be secured to the PMC motherboard using M2.5 screws in the four holes provided. The PMC bezel through which the I/O connectors protrude should be flush with the front panel of the PMC motherboard.

2.4. Installing the ADM-XRC-5T-DA1 if fitted to an ADC-PMC

The ADM-XRC-5T-DA1 can be supplied for use in standard PC systems fitted to an ADC-PMC carrier board. The ADC-PMC can support up to two PMC cards whilst maintaining host PC PCI compatibility. If you are using a ADC-PMC refer to the supplied documentation for information on jumper settings. All that is required for installation is a PCI slot that has enough space to accommodate the full-length card. The ADC-PMC is compatible with 5V and 3V PCI (32 and 64 bit) and PCI-X slots.

It should be noted that the ADC-PMC uses a standard bridge to provide a secondary PCI bus for the ADM-XRC-5T-DA1 and that some older BIOS code does not set up these devices correctly. Please ensure you have the latest version of BIOS appropriate for your machine.

3. Software Installation

Please refer to the SDK installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing. The standard SDK routines info.exe, clock.exe, itest.exe, dma.exe and memory.exe are all supported by this board and can be used as templates for designs.

In addition, example code for data acquisition and generation is provided separately to the SDK routines.

4. Board Description

The ADM-XRC-5T-DA1 follows the architecture of the ADM-XRC series and decouples the "target" FPGA from the PCI interface, allowing user applications to be designed with minimum effort and without the complexity of PCI design.

A separate Bridge / Control FPGA interfaces to the PCI bus and provides a simpler Local Bus interface to the target FPGA. It also performs all of the board control functions including the configuration of the target FPGA, programmable clock setup and the monitoring of on-board voltage and temperature.

DDR2 SDRAM, SSRAM and serial flash memory connect to the target FPGA and are supported by Xilinx or third party IP.

Analogue IO capability is provided by replacing the ADM-XRC-5T1 front i/o connector with hard-wired routeing to analogue circuitry embedded in the board.

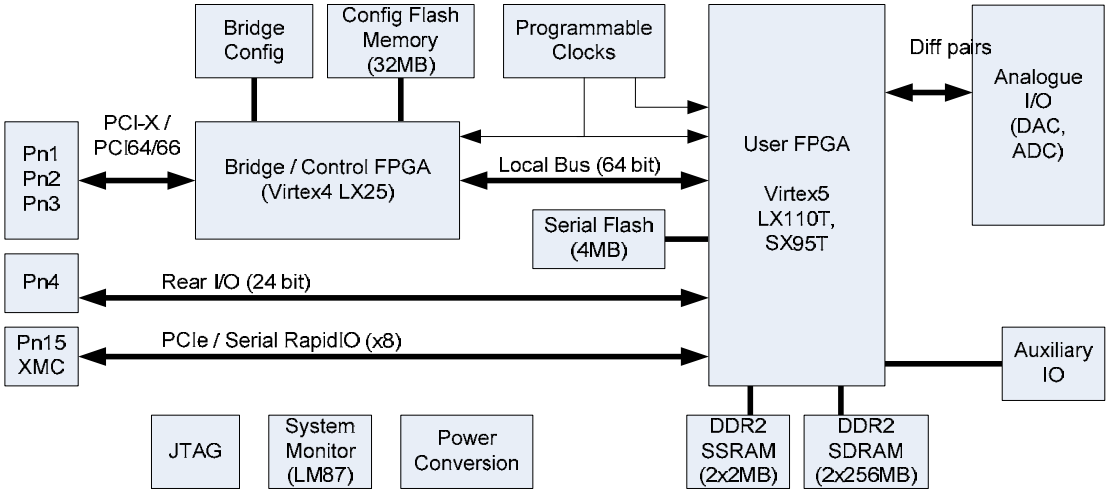


Figure 1 ADM-XRC-5T-DA1 Block Diagram

4.1. Local Bus

The ADM-XRC-5T-DA1 implements a multi-master local bus between the bridge and the target FPGA using a 32-bit multiplexed address and data path. The bridge design is asynchronous and allows the local bus to be run faster or slower than the PCI bus clock to suit the requirements of the user design.

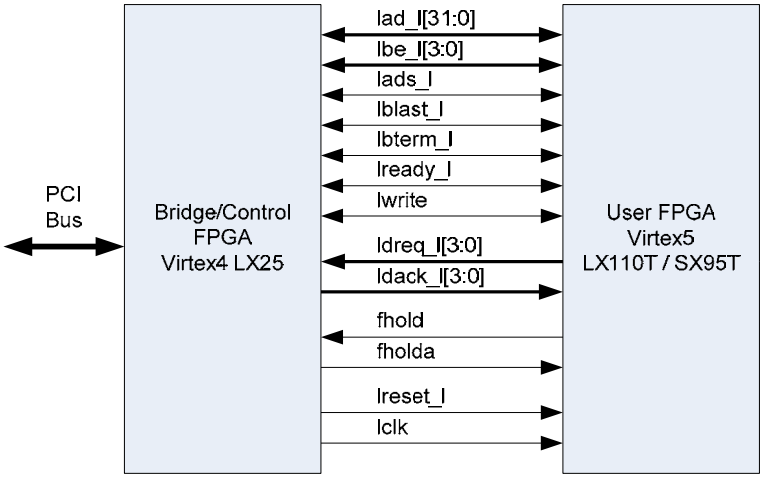


Figure 2 Local Bus Interface

Signal	Type	Purpose
lad[0:31]	bidir	Address and data bus.
lbe_l[0:3]	bidir	Byte qualifiers
lads_l	bidir	Indicates address phase
lblast_l	bidir	Indicates last word
lbterm_l	bidir	Indicates ready and requests new address phase
lready_l	bidir	Indicates that target accepts or presents new data
lwrite	bidir	Indicates a write transfer from master
ldreq_l[0:3]	unidir	DMA request from target to bridge
ldack_l[0:3]	unidir	DMA acknowledge from bridge to target
fhold	unidir	Target bus request
fholda	unidir	Bridge bus acknowledge
lreset_l	unidir	Reset to target
lclk	unidir	Clock to synchronise bridge and target

Table 1 Local Bus Interface Signal List

4.2. Flash Memory

The ADM-XRC-5T-DA1 is fitted with two separate Flash memories: one connected to the Bridge / Control FPGA and the other to the User FPGA.

4.2.1. Board Control Flash

An Intel PC28F256P30 flash memory is used for storing a configuration bitstream for the User FPGA. Once the Bridge / Control FPGA is configured, it checks for a valid bitstream in flash and, if present, automatically loads it into the User FPGA. This process can be inhibited by setting a jumper on the JTAG connector. See the description of the "FBS" signal in Section 4.4 for further information.

Access to this flash device is only possible through control logic registers. The flash is not directly mapped onto the local bus.

Programming, erasing and verification of the flash are supported by the ADM-XRC SDK and driver. Utilities are provided to load bitstreams into the flash. These also verify the bitstream is compatible with the target FPGA.

4.2.2. User FPGA Flash

An ST M25P32 flash memory with SPI interface is connected to the User FPGA for the storage of application-specific information.

4.3. Health Monitoring

The ADM-XRC-5T-DA1 has the ability to monitor temperature and voltage of key parts of the board to maintain a check on the operation of the board. The monitoring is implemented by a National Semiconductor LM87 and is supported by the board control logic connected using I^2C.

The Control Logic scans the LM87 when instructed by host software and stores the current voltage and temperature measurements in a blockram. This allows the values to be read without the need to communicate directly with the monitor.

The following supplies and temperatures, as shown in Table 2, are monitored.

Monitor	Purpose
1.0V	User FPGA Core Supply
1.2V	Bridge FPGA Core Supply
1.8V	Memories, User FPGA Memory I/O, Local Bus I/O Config CPLD Core Supply
2.5V	Source voltage for Front, Rear I/O
3.3V	Board Input Supply
5.0V	Board Input Supply
Pn4_VCCIO	Either 2.5V or 3.3V Rear (Pn4) I/O Voltage
XRM_VCCIO	Either 2.5V or 3.3V Front Panel I/O Voltage
Temp1	User FPGA die temperature
Temp2	LM87 on die temperature for board/ambient

Table 2 Voltage and Temperature Monitors

An application is provided in the SDK that permits the reading of the health monitor. The typical output of the monitor is shown below, provided by the SYSMON program.

```
*** SysMon ***

FPGA    Space Base Adr = 00900000
Control Space Base Adr = 00d00000


+1V0 Reading = 1.01 V
+1V2 Reading = 1.21 V
+1V8 Reading = 1.81 V
+2V5 Reading = 2.51 V
+3V3 Reading = 3.32 V
+5V  Reading = 5.04 V
Pn4  Reading = 3.31 V
FPIO Reading = 3.34 V

SysMon Int Temp =   33 deg. C
User FPGA Temp  =   26 deg. C
```

4.4. JTAG

A JTAG header is provided to allow download of the FPGA using the Xilinx tools and serial download cables. This also allows the use of ChipScope PRO ILA to debug an FPGA design. It should be noted that four devices will be detected when the SCAN chain is initialised.

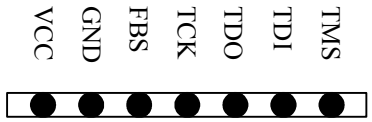


Figure 3 JTAG Header

The VCC supply provided on J5 to the JTAG cable is +2.5V and is protected by a poly fuse with a rating of 350mA.

FBS

The FBS signal is an input to the control logic and provides control of the cold boot process. By default with no link fitted, the control logic will load a bitstream from flash into the FPGA if one is present. Shorting FBS to the adjacent GND pin will disable this process and can be used to recover situations where rogue bitstreams have been stored in flash.

4.5. Clocks

The ADM-XRC-5T-DA1 is provided with numerous clock sources, as shown in Figure 4 below:

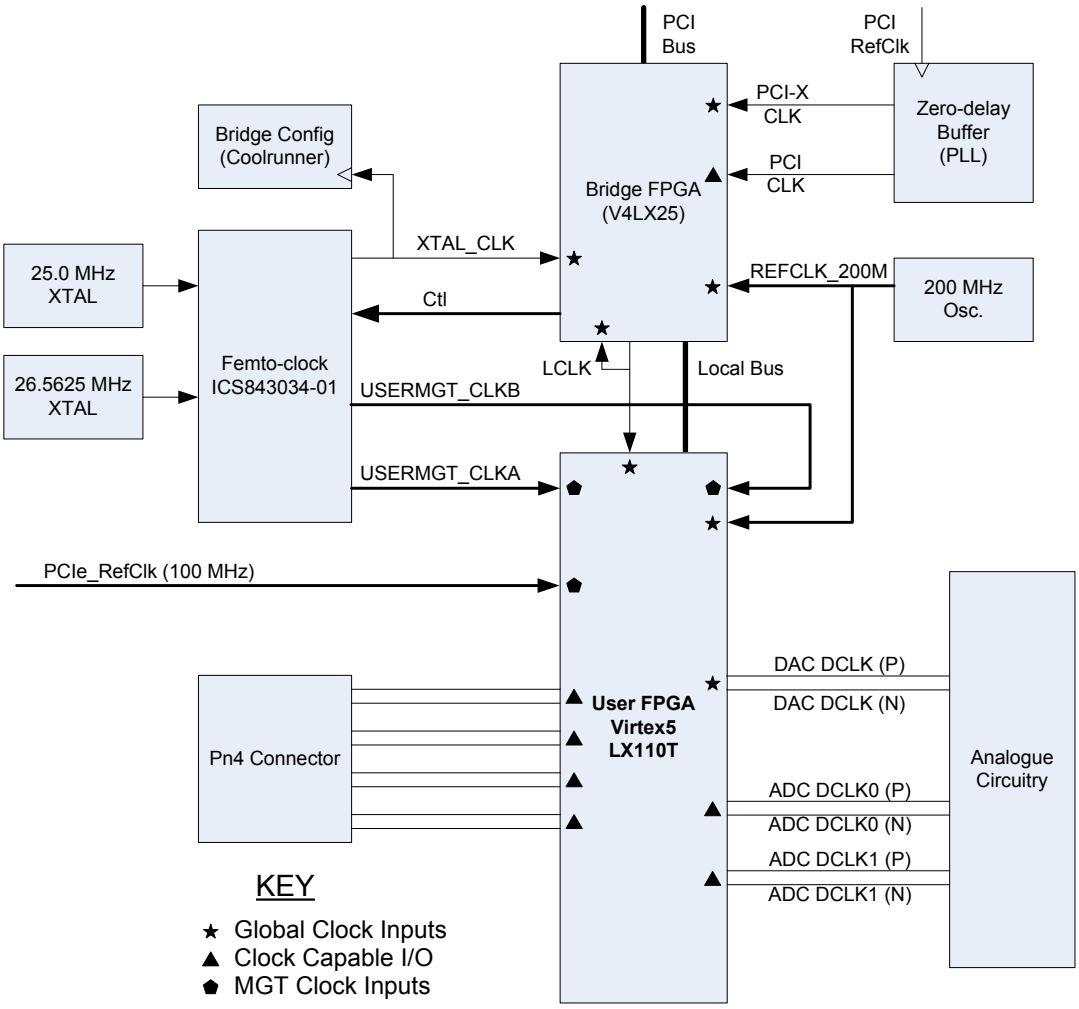


Figure 4 Clock Structure

4.5.1. LCLK

The Local Bus can be used at up to 80 MHz and all timing is synchronised to LCLK between the Bridge and User FPGAs. LCLK is generated from a 200MHz reference by a DCM within the bridge FPGA. The minimum LCLK frequency (determined by the DCM specification) is 32MHz.

The LCLK frequency is set by writing to the board control logic. (See SDK for details and example application).

Note: If the user FPGA application includes a DCM driven by LCLK (or one of the other programmable clocks), the clock frequency should be set prior to FPGA configuration.

4.5.2. REFCLK

In order to make use of the IODELAY features of Virtex™-5, a stable low-jitter clock source is required to provide the base timing for tap delay lines in each IOB in the User FPGA. The ADM-XRC-5T-DA1 is fitted with a 200MHz LVPECL (LVDS optional) oscillator connected to global clock resource pins. This reference clock can also be used for application logic if required.

4.5.3. PCIe Reference Clock

A 100MHz PCIe reference clock input from the Primary XMC connector (Pn15) is connected to one of the dedicated MGT clock inputs on the user FPGA. (See Table 3 for details of the MGT clock connections.)

4.5.4. User MGT Clocks

A programmable, low-jitter clock source is provided by an ICS843034-01 “FemtoClocks” frequency synthesiser. The synthesiser has two source crystals – one at 26.5625MHz (for Fibre Channel applications) and another at 25.0MHz (suitable for PCIe, Gigabit Ethernet etc.). The synthesiser also has two clock outputs.

”USERMGT_CLKA” is connected to an MGT clock input on the top-half of the user FPGA. It may be used as an alternative to the PCIe reference for the MGTs connected to the Primary XMC.

”USERMGT_CLKB” is connected to an MGT clock input on the bottom half of the user FPGA. It may be used as the reference for the front user MGTs. (See Table 3 for details of the MGT clock connections.)

Note: Either of these clocks can provide a programmable source for applications that do not use MGTs.

Clock Name	GTP No.	FPGA Pin (P/N)	Reference for:
PCIE_REFCLK	114	Y4 / Y3	Primary XMC (Pn15) MGTs
USERMGT_CLKA	122	AL5 / AL4	Primary XMC (Pn15) MGTs
USERMGT_CLKB	112	P4 / P3	Front (CN2) user MGTs

Table 3 MGT Clock Connections

4.5.5. DAC Global Clock Input

The DAC data clock is routed to a global clock input and then fed back externally to a second global clock input to provide data deskewing.

Clock Name	FPGA Pin (P/N)	Comment
DAC_DCLK	AF18 / AE18	Global input
DAC_DCLK_FB	P31 /P30	Output
DAC_DCLK_FBIN	AH17 / AG16	Global input

Table 4 DAC DCLK Connections

ADC Regional Clocks

The data clock from the ADC is split into two copies, each of which drives a regional clock input. Adjacent banks are used to allow the use of BUFIO on both banks to capture the data but a single BUFR from either clock input to be used as the fabric clock.

ADC Clocks	FPGA Bank	Pins
DCLK_13 (p,n)	13	AH34, AJ34
DCLK_17 (p,n)	17	AB30, AC30

Table 5 ADC Regional Clocks

4.5.6. PCI Clocks

The PCI Interface within the bridge FPGA requires a regional clock input for 66MHz PCI operation or a global clock input for PCI-X. To comply with the single-load requirement in the PCI specification, a zero-delay clock buffer is used to route the PCI clock to the two different clock inputs.

The clock buffer has a PLL with a minimum input frequency of 24MHz, potentially causing problems in applications that use the PCI 33MHz mode with a slow clock. In this case, the buffer can be bypassed to provide full PCI 33MHz compatibility.

4.6. User FPGA

4.6.1. Configuration

The ADM-XRC-5T-DA1 performs configuration from the host at high speed using SelectMAP. The FPGA may also be configured from flash or by JTAG via header J2.

Download from the host is the fastest way to configure the User FPGA with 8 bit SelectMAP mode enabled. This permits an ideal configuration speed of up to 40MB/s.

The ADM-XRC-5T-DA1 can be configured to boot the User FPGA from flash on power-up if a valid bit-stream is detected in the flash. Booting from flash will also configure the programmable clocks.

4.6.2. I/O Bank Voltages

Bank	Voltage	Description
0	2.5V	Configuration I/F
1	1.8V	SSRAM
2	1.8V	SelectMAP I/F
3	1.8V	SSRAM
4	2.5V	Clocks, Serial Flash
5	1.8V	SSRAM
6	1.8V	DDRII SRAM
11	2.5V	DAC
12	1.8V	Local Bus
13	2.5V	ADC
15	2.5V	DAC
17	2.5V	ADC
18	3V3	Pn4 Interface
19	2.5V	DAC
20	1.8V	Local Bus
21	1.8V	DDRII DRAM
22	1.8V	DDRII DRAM
23	1.8V	SSRAM
25	1.8V	DDRII DRAM

Table 6 User FPGA I/O Bank Voltages

4.6.3. Memory Interfaces

The ADM-XRC-5T-DA1 has two banks of DDRII SDRAM. These banks consist of two memory devices in parallel to provide a 32 bit datapath. 1Gb Micron MT47H64M16 devices are fitted as standard to provide 256MB per bank. The board will support higher capacity devices as and when they become available.

The ADM-XRC-5T-DA1 has been designed for compatibility with Xilinx memory interface cores. (read_en_out / read_en_in is an external loopback signal.)

Details of the signalling standards are given in the table below:

Name	Direction	I/O Standard
DDR_ad[15:0], DDR_ba[2:0], DDR_rasn, DDR_casn, DDR_wen, DDR_csn, DDR_cke, DDR_odt	Output	SSTL18_I_DCI
DDR_ck0, DDR_ckn0	Output	DIFF_SSTL18_II
DDR_dq[15:0]	BiDir	SSTL18_II
DDR_dm[1:0]	Output	SSTL18_II_DCI
DDR_dqs[1:0], DDR_dqsn[1:0]	BiDir	DIFF_SSTL18_II
DDR_ck1, DDR_ckn1	Output	DIFF_SSTL18_II
DDR_dq[31:16]	BiDir	SSTL18_II
DDR_dm[3:2]	Output	SSTL18_II_DCI
DDR_dqs[3:2], DDR_dqsn[3:2]	BiDir	DIFF_SSTL18_II

Table 7 DDR Memory Bank Configuration

4.7. Analogue Section Interface

Signal	FPGA Pin	Comment
adc_dckx_n	aj34	Bank 13 clock
adc_dckx_p	ah34	Bank 13 clock
adc_dcky_n	ac30	Bank 17 clock
adc_dcky_p	ab30	Bank 17 clock
adc_ovr_n	ah33	Bank No 13
adc_ovr_p	ag33	Bank No 13
idatadel_p(0)	af33	Bank No 13
idatadel_n(0)	ae33	Bank No 13
idatadel_p(1)	af34	Bank No 13
idatadel_n(1)	ae34	Bank No 13
idatadel_p(2)	ad32	Bank No 13
idatadel_n(2)	ae32	Bank No 13
idatadel_p(3)	aj32	Bank No 13
idatadel_n(3)	ak32	Bank No 13
idatadel_p(4)	ak34	Bank No 13
idatadel_n(4)	ak33	Bank No 13
idatadel_p(5)	al34	Bank No 13
idatadel_n(5)	al33	Bank No 13
idatadel_p(6)	an34	Bank No 13
idatadel_n(6)	an33	Bank No 13
idatadel_p(7)	am33	Bank No 13
idatadel_n(7)	am32	Bank No 13
idata_p(0)	an32	Bank No 13
idata_n(0)	ap32	Bank No 13
idata_p(1)	aa29	Bank No 17
idata_n(1)	aa30	Bank No 17
idata_p(2)	ac32	Bank No 13
idata_n(2)	ab32	Bank No 13
idata_p(3)	ab31	Bank No 17
idata_n(3)	aa31	Bank No 17
idata_p(4)	ad30	Bank No 17
idata_n(4)	ac29	Bank No 17
idata_p(5)	ae29	Bank No 17
idata_n(5)	ad29	Bank No 17
idata_p(6)	af29	Bank No 17
idata_n(6)	af30	Bank No 17
idata_p(7)	aj31	Bank No 17
idata_n(7)	ak31	Bank No 17
qdata_p(0)	w31	Bank No 17
qdata_n(0)	y31	Bank No 17
qdata_p(1)	w29	Bank No 17
qdata_n(1)	v29	Bank No 17
qdata_p(2)	w24	Bank No 17
qdata_n(2)	v24	Bank No 17
qdata_p(3)	y27	Bank No 17
qdata_n(3)	w27	Bank No 17
qdata_p(4)	w34	Bank No 13
qdata_n(4)	v34	Bank No 13
qdata_p(5)	aa34	Bank No 13
qdata_n(5)	y34	Bank No 13
qdata_p(6)	aj30	Bank No 17
qdata_n(6)	ah30	Bank No 17
qdata_p(7)	ah29	Bank No 17
qdata_n(7)	ag30	Bank No 17
qdatadel_p(0)	v32	Bank No 13
qdatadel_n(0)	v33	Bank No 13
qdatadel_p(1)	ac34	Bank No 13
qdatadel_n(1)	ad34	Bank No 13

qdatadel_p(2)	v25	Bank No 17
qdatadel_n(2)	w25	Bank No 17
qdatadel_p(3)	y28	Bank No 17
qdatadel_n(3)	y29	Bank No 17
qdatadel_p(4)	ac33	Bank No 13
qdatadel_n(4)	ab33	Bank No 13
qdatadel_p(5)	v28	Bank No 17
qdatadel_n(5)	v27	Bank No 17
qdatadel_p(6)	y26	Bank No 17
qdatadel_n(6)	w26	Bank No 17
qdatadel_p(7)	y33	Bank No 13
qdatadel_n(7)	aa33	Bank No 13

Table 8 ADC Interface

Signal	**FPGA Pin**	**Comment**
dac_dclk_p	af18	Dclk from DAC to FPGA
dac_dclk_n,	ae18	Dclk from DAC to FPGA
dac_dclk_fb_n	p30	DAC Clock loopback output,LVDS
dac_dclk_fb_p	p31	DAC Clock loopback output,LVDS
dac_dclk_fbin_n	ag16	Global clock input feedback to DCM
dac_dclk_fbin_p	ah17	Global clock input feedback to DCM
dac_cal	n24	DAC Control (single ended)
dac_delay	p27	DAC Control (single ended)
dac_rf	t24	DAC Control (single ended)
dac_rz	p25	DAC Control (single ended)
dacdat_a_n(0)	f26	Bank 19
dacdat_a_p(0)	f25	Bank 19
dacdat_a_n(1)	h24	Bank 19
dacdat_a_p(1)	h25	Bank 19
dacdat_a_n(2)	d32	Bank 11
dacdat_a_p(2)	c32	Bank 11
dacdat_a_n(3)	t25	Bank 15
dacdat_a_p(3)	u25	Bank 15
dacdat_a_n(4)	m26	Bank 19
dacdat_a_p(4)	m25	Bank 19
dacdat_a_n(5)	a33	Bank 11
dacdat_a_p(5)	b32	Bank 11
dacdat_a_n(6)	u28	Bank 15
dacdat_a_p(6)	u27	Bank 15
dacdat_a_n(7)	g26	Bank 19
dacdat_a_p(7)	g25	Bank 19
dacdat_a_n(8)	t26	Bank 15
dacdat_a_p(8)	u26	Bank 15
dacdat_a_n(9)	r31	Bank 15
dacdat_a_p(9)	t31	Bank 15
dacdat_a_n(10)	t29	Bank 15
dacdat_a_p(10)	t28	Bank 15
dacdat_a_n(11)	t34	Bank 15
dacdat_a_p(11)	u33	Bank 15
dacdat_b_n(0)	j26	Bank 19
dacdat_b_p(0)	j27	Bank 19
dacdat_b_n(1)	m27	Bank 19
dacdat_b_p(1)	n27	Bank 19
dacdat_b_n(2)	e31	Bank 15
dacdat_b_p(2)	f31	Bank 15
dacdat_b_n(3)	l24	Bank 19
dacdat_b_p(3)	k24	Bank 19
dacdat_b_n(4)	f30	Bank 15
dacdat_b_p(4)	g30	Bank 15
dacdat_b_n(5)	j29	Bank 15
dacdat_b_p(5)	h29	Bank 15

dacdat_b_n(6)	f29	Bank 15
dacdat_b_p(6)	e29	Bank 15
dacdat_b_n(7)	f28	Bank 19
dacdat_b_p(7)	e28	Bank 19
dacdat_b_n(8)	g28	Bank 19
dacdat_b_p(8)	h28	Bank 19
dacdat_b_n(9)	h27	Bank 19
dacdat_b_p(9)	g27	Bank 19
dacdat_b_n(10)	j25	Bank 19
dacdat_b_p(10)	j24	Bank 19
dacdat_b_n(11)	e27	Bank 19
dacdat_b_p(11)	e26	Bank 19
dacdat_c_n(0)	l31	Bank 15
dacdat_c_p(0)	k31	Bank 15
dacdat_c_n(1)	k32	Bank 11
dacdat_c_p(1)	k33	Bank 11
dacdat_c_n(2)	h33	Bank 11
dacdat_c_p(2)	j32	Bank 11
dacdat_c_n(3)	e33	Bank 11
dacdat_c_p(3)	e32	Bank 11
dacdat_c_n(4)	m30	Bank 15
dacdat_c_p(4)	l30	Bank 15
dacdat_c_n(5)	j31	Bank 15
dacdat_c_p(5)	j30	Bank 15
dacdat_c_n(6)	j34	Bank 11
dacdat_c_p(6)	h34	Bank 11
dacdat_c_n(7)	f34	Bank 11
dacdat_c_p(7)	g33	Bank 11
dacdat_c_n(8)	d34	Bank 15
dacdat_c_p(8)	c34	Bank 15
dacdat_c_n(9)	e34	Bank 11
dacdat_c_p(9)	f33	Bank 11
dacdat_c_n(10)	c33	Bank 11
dacdat_c_p(10)	b33	Bank 11
dacdat_c_n(11)	g31	Bank 15
dacdat_c_p(11)	h30	Bank 15
dacdat_d_n(0)	r34	Bank 11
dacdat_d_p(0)	t33	Bank 11
dacdat_d_n(1)	r32	Bank 11
dacdat_d_p(1)	r33	Bank 11
dacdat_d_n(2)	n28	Bank 19
dacdat_d_p(2)	m28	Bank 19
dacdat_d_n(3)	n32	Bank 11
dacdat_d_p(3)	p32	Bank 11
dacdat_d_n(4)	n30	Bank 15
dacdat_d_p(4)	m31	Bank 15
dacdat_d_n(5)	r27	Bank 15
dacdat_d_p(5)	r26	Bank 15
dacdat_d_n(6)	p29	Bank 15
dacdat_d_p(6)	n29	Bank 15
dacdat_d_n(7)	l26	Bank 19
dacdat_d_p(7)	l25	Bank 19
dacdat_d_n(8)	l28	Bank 19
dacdat_d_p(8)	k28	Bank 19
dacdat_d_n(9)	m32	Bank 11
dacdat_d_p(9)	l33	Bank 11
dacdat_d_n(10)	k26	Bank 19
dacdat_d_p(10)	k27	Bank 19
dacdat_d_n(11)	u31	Bank 11
dacdat_d_p(11)	u32	Bank 11

Table 9 DAC Interface

4.8. Pn4 I/O

Up to 12 pairs of differential or 24 single-ended signals are available on Pn4 and are sourced from Bank 18 of the User FPGA. All of the signal traces are routed as 100 Ohm differential pairs and each pair is matched in length. The worst case difference in trace length between any two pairs is 10mm.

Signal	FPGA Pin	Comment
pn4_p(1)	ab6	Bank 18
pn4_n(1)	ab7	Bank 18
pn4_p(2)	ac7	Bank 18
pn4_n(2)	ad7	Bank 18
pn4_p(3)	y8	Bank 18
pn4_n(3)	y9	Bank 18
pn4_p(4)	aa6	Bank 18
pn4_n(4)	y7	Bank 18
pn4_p(5)	y11	Bank 18
pn4_n(5)	w11	Bank 18
pn4_p(6)	ah7	Bank 18
pn4_n(6)	ag7	Bank 18
pn4_p(7)	w6	Bank 18
pn4_n(7)	y6	Bank 18
pn4_p(8)	ae7	Bank 18
pn4_n(8)	af6	Bank 18
pn4_p(9)	w7	Bank 18
pn4_n(9)	v7	Bank 18
pn4_p(10)	w10	Bank 18
pn4_n(10)	w9	Bank 18
pn4_p(11)	v8	Bank 18
pn4_n(11)	u8	Bank 18
pn4_p(12)	v10	Bank 18
pn4_n(12)	v9	Bank 18

Table 10 Pn4 to FPGA Assignments

4.8.1. Pn4 Signalling Voltage

The signalling voltage on the Pn4 connector is selectable by switch SW1B.

Switch 1B	Pn4 voltage
Open	2.5V
Closed	3.3V

Table 11 Pn4 I/O Voltage Selection

It should be noted that the switch does not directly route power. The switch position is monitored by the board control logic which, in turn, sets a power multiplexer to be either 2.5V or 3.3V.

4.9. XMC Interface

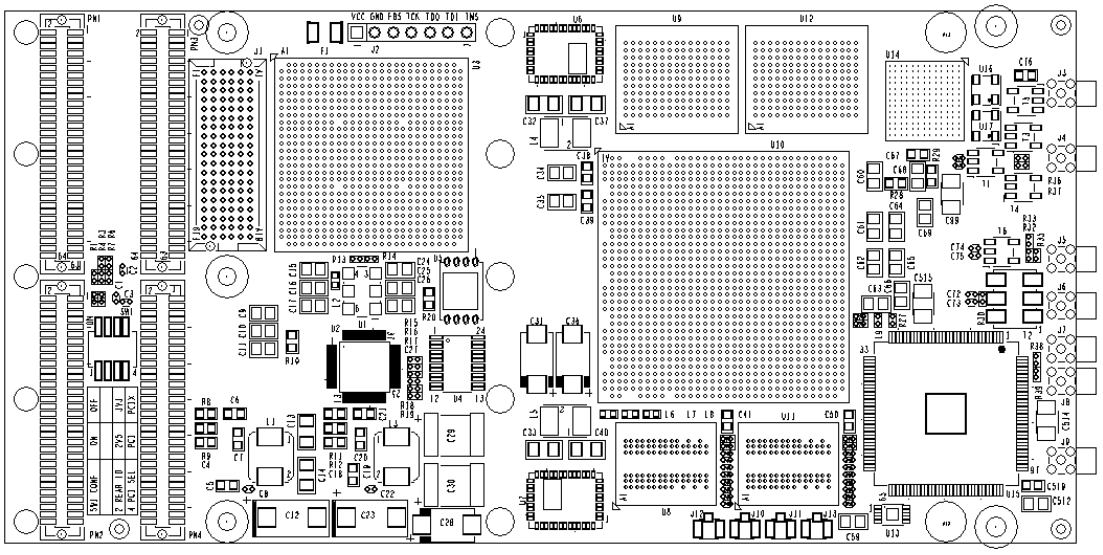
4.9.1. Primary XMC Connector, P15

The MGT (GTP) links connected between the user FPGA and the Primary XMC connector, P15, are compatible with PCI Express and Serial RapidIO. Depending upon the carrier card, they may also be used for user-specific applications.

Signal	FPGA Pin	GTP Number	Location (LX110T / SX95T)	P15 Pin
PCIE_TX0_P	AN5	126A	GTP_DUAL_X0Y0	A1
PCIE_TX0_N	AN6	"	"	B1
PCIE_RX0_P	AP6	"	"	A11
PCIE_RX0_N	AP7	"	"	B11
PCIE_TX1_P	AN10	126B	"	D1
PCIE_TX1_N	AN9	"	"	E1
PCIE_RX1_P	AP9	"	"	D11
PCIE_RX1_N	AP8	"	"	E11
PCIE_TX2_P	AK2	122A	GTP_DUAL_X0Y1	A3
PCIE_TX2_N	AL2	"	"	B3
PCIE_RX2_P	AL1	"	"	A13
PCIE_RX2_N	AM1	"	"	B13
PCIE_TX3_P	AN4	122B	"	D3
PCIE_TX3_N	AN3	"	"	E3
PCIE_RX3_P	AP3	"	"	D13
PCIE_RX3_N	AP2	"	"	E13
PCIE_TX4_P	AD2	118A	GTP_DUAL_X0Y2	A5
PCIE_TX4_N	AE2	"	"	B5
PCIE_RX4_P	AE1	"	"	A15
PCIE_RX4_N	AF1	"	"	B15
PCIE_TX5_P	AJ2	118B	"	D5
PCIE_TX5_N	AH2	"	"	E5
PCIE_RX5_P	AH1	"	"	D15
PCIE_RX5_N	AG1	"	"	E15
PCIE_TX6_P	V2	114A	GTP_DUAL_X0Y3	A7
PCIE_TX6_N	W2	"	"	B7
PCIE_RX6_P	W1	"	"	A17
PCIE_RX6_N	Y1	"	"	B17
PCIE_TX7_P	AC2	114B	"	D7
PCIE_TX7_N	AB2	"	"	E7
PCIE_RX7_P	AB1	"	"	D17
PCIE_RX7_N	AA1	"	"	E17

Table 12 XMC P15 Connections

5. Board Layout



Reference	Function	Note
J3	DAC out	50 R
J4	DAC Clock in	50 R
J5	ADC in	50 R
J6	ADC Clock in	50 R
J7	Trig Diff p	High speed diff trigger pair, p
J8	Trig Diff n	High speed diff trigger pair, n
J9	Aux/GPIO	LVTTL I/O

Table 13 Board Connectors

6. Revision History

Date	Revision	Nature of Change
1-06-2008	1.0	First Release.
15-08-09	1.1	Minor typo corrections