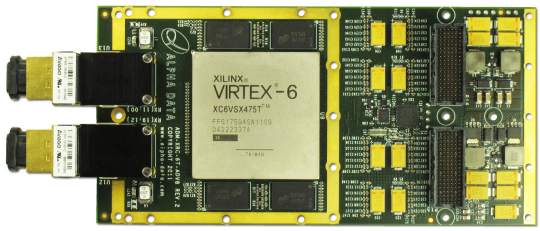
ADM-XRC-6T-ADV8

ALPHA DATA

8th May 2012 **Datasheet Revision: 1.1**



Summary

The **ADM-XRC-6T-ADV8** is a high performance reconfigurable XMC (VITA 42.3 Mezzanine Card) based on the Xilinx™ Virtex-6 LXT and SXT ranges of Platform FPGAs. Features include PCI Express® Gen2 interface, external memory, eight JPEG2000 compression devices, High Speed Optical Interface, temperature monitoring and flash boot facilities.
A comprehensive cross platform API with support for **Microsoft Windows™**, **Linux** and **VxWorks** provides access to the full functionality of these hardware features.

Features

8 JPEG2000 compression devices
High Speed Optical Interfaces

Applications:

Image/Video Processing

Target Devices:

Xilinx Virtex-6 - LX550T, SX475T (FFG1759)

Memory:

SDRAM - 1GByte in 4 independent banks (2GByte option) of DDR3 SDRAM @ 800MT/s (32-bit wide so 3.2GB/s)

FLASH - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.

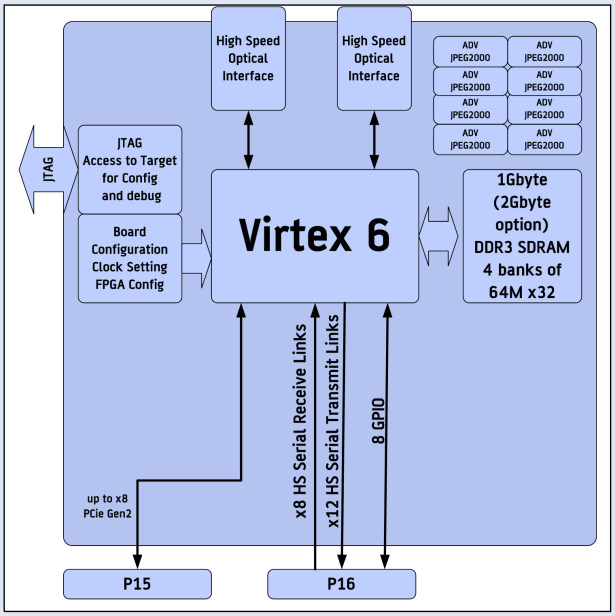
Front Connector I/O:

20 High-Speed Optical Receiver Links

Rear Connector I/O:

8 High-Speed Serial Links via P15 connector (allowing second x4 PCI Express® Gen 2 channel from FPGA)
8 High-Speed Serial Receive links via P16 Connector
12 High-Speed Serial Transmit links via P16 Connector

8 LVTTL GPIO connections via P16 connector



ADM-XRC-6T-ADV8

Specification	
Product Name	ADM-XRC-6T-ADV8
Target Devices	Xilinx Virtex-6 - LX550T, SX475T (FFG1759)
Host I/F	PCI Express® Gen2 x4
Interface	PCI Express® Gen2 x1, x2, x4 or x8 link direct to FPGA 4 DMA Controllers Interrupt Controller
Memory	**SDRAM** - 1GByte in 4 independent banks (2GByte option) of DDR3 SDRAM @ 800MT/s (32-bit wide so 3.2GB/s) **FLASH** - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.
Front I/O	20 High-Speed Optical Receiver Links
Rear I/O	8 High-Speed Serial Links via P15 connector (allowing second x4 PCI Express® Gen 2 channel from FPGA) 8 High-Speed Serial Receive links via P16 Connector 12 High-Speed Serial Transmit links via P16 Connector 8 LVTTL GPIO connections via P16 connector
Clocks	Low-jitter 156.25MHz reference clock, suitable for GTX links Low-jitter 200MHz reference clock for GCLK, IOBs etc.
Device Configuration	From Flash direct on power up External JTAG connector
Software	Drivers for Microsoft Windows™, Linux and VxWorks The ADM-XRC Gen3 SDK provides the example C and HDL source code, giving software engineers and FPGA designers a head start in creating applications.
Environmental	**Temperature:** **Air cooled option (AC0)** Operating Temperature 0° to +55°C **Air cooled Extended Range (ACE)** Operating Temperature 0° to +55°C **Air cooled industrial option (AC1)** Operating Temperature -20° to +55°C **Conduction cooled option (CC1)** Operating Temperature -40° to 71°C **EMC:** FCC 47CFR Part 2 EN55022 Equipment Class B

Ordering Codes		
ADM-XRC-6T-ADV8/z-y(m)(c)		
Virtex-6 device	z	LX550T, SX475T
Virtex-6 speed	y	1, 2, 3
Memory Size Fitted	m	blank = 256MBytes per bank - 1GBytes for the board, /2 =s512MBytes per bank - 2GBytes for the board
Cooling	c	blank = air cooled commercial, /AC1 = air cooled industrial, /CC1 = conduction cooled industrial
Note	#	not all FPGA speed grades available in all configurations. Contact Alpha Data for full details.

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