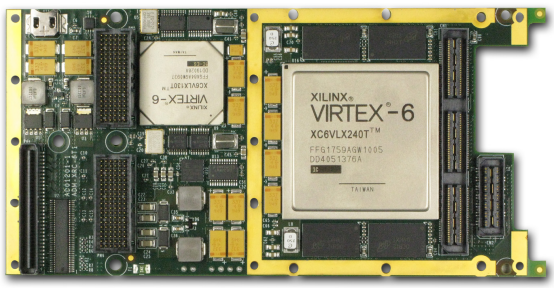
ADM-XRC-6TGE

4th February 2014 **Datasheet Revision: 1.1**



Summary

The **ADM-XRC-6TGE** is a high performance reconfigurable XMC (VITA 42.3 Mezzanine Card) based on the Xilinx™ Virtex-6 LXT and SXT ranges of Platform FPGAs. Features include PCI Express® Gen2 interface, external memory, high density I/O, temperature monitoring, battery backed encryption and flash boot facilities.
A 10/100/1000Base-T Ethernet interface to the target FPGA is provided through the rear Pn6 connector.
A comprehensive cross platform API with support for **Microsoft Windows™**, **Linux** and **VxWorks** provides access to the full functionality of these hardware features.
The optional fitting of the Pn4 connector provides an additional 64 General Purpose IO (GPIO) links to the carrier card.

Features

Applications:

Radar/Sonar Beamforming
ELINT
Image/Video Processing
Data Encryption

Target Devices:

Xilinx Virtex-6 - LX240T, LX365T, LX550T, SX315T, SX475T (FFG1759)

Memory:

SDRAM - 1GByte in 4 independent banks (2GByte/4GByte options) of DDR3 SDRAM @ 800MT/s (32-bit wide so 3.2GB/s)

FLASH - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.

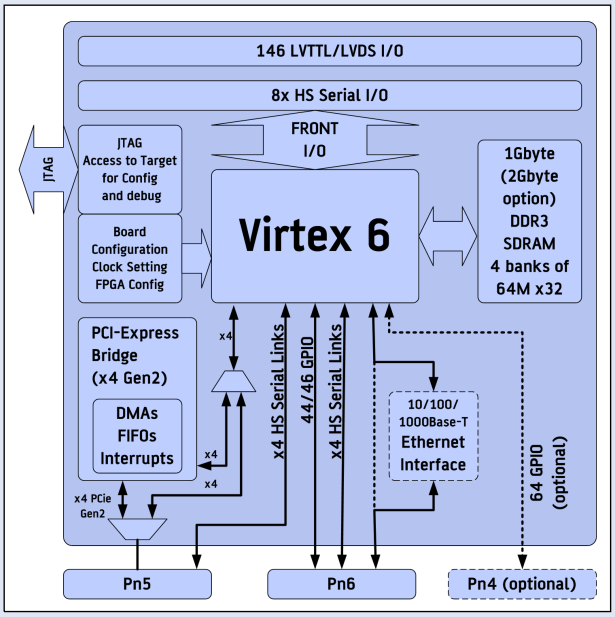
Front Connector I/O:

Up to 146 LVCMOS/LVDS I/O
Programmable signaling levels of 1.5V, 1.8V or 2.5V

8 High-Speed Serial Links

Rear Connector I/O:

Pn5
x4 PCIe to Bridge FPGA or Target FPGA, x4 PCIe to Target FPGA, JTAG, I2C
Pn6
x4 MGT to Target FPGA, x4 MGT to Target FPGA **or** 10/100/1000Base-T to magnetics and Gigabit Ethernet PHY. (MAC to PHY Interface is SGMII), External MGT reference clock **or** 2 GPIO (Can be used single-ended **or** as 1 differential pair), 44 GPIO (Can be used single-ended **or** as 22 differential pairs)
Pn4
64 GPIO (Can be used single-ended **or** as 32 differential pairs)



ADM-XRC-6TGE

ALPHA DATA

Specification

Product Name	ADM-XRC-6TGE
Target Devices	Xilinx Virtex-6 - LX240T, LX365T, LX550T, SX315T, SX475T (FFG1759)
Host I/F	PCI Express® Gen2 x4
Interface	PCI Express® Gen2 x1, x2 or x4 link to separate bridge device with 2GB/s local link to user FPGA 4 DMA Controllers Interrupt Controller
Memory	**SDRAM** - 1GByte in 4 independent banks (2GByte/4GByte options) of DDR3 SDRAM @ 800MT/s (32-bit wide so 3.2GB/s) **FLASH** - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.
Front I/O	Up to 146 LVCMOS/LVDS I/O Programmable signaling levels of 1.5V, 1.8V or 2.5V 8 High-Speed Serial Links
XRM2	The ADM-XRC-6TGE is also available for XRM2 based FPGA products.
Rear I/O	**Pn5** x4 PCIe to Bridge FPGA or Target FPGA, x4 PCIe to Target FPGA, JTAG, I2C **Pn6** x4 MGT to Target FPGA, x4 MGT to Target FPGA **or** 10/100/1000Base-T to magnetics and Gigabit Ethernet PHY. (MAC to PHY Interface is SGMII), External MGT reference clock **or** 2 GPIO (Can be used single-ended **or** as 1 differential pair), 44 GPIO (Can be used single-ended **or** as 22 differential pairs) **Pn4** 64 GPIO (Can be used single-ended **or** as 32 differential pairs)
Clocks	Low-jitter 250MHz reference clock, suitable for SerDes applications Low-jitter 200MHz reference clock for IOB delay circuits Custom clock inputs available through the XRM interface 3 Further User-Programmable Clocks for custom applications
Device Configuration	PCI Express® direct to SelectMAP port From Flash direct on power up External JTAG connector
Software	Drivers for Microsoft Windows™, Linux and VxWorks The ADM-XRC Gen3 SDK provides the example C and HDL source code, giving software engineers and FPGA designers a head start in creating applications.
Battery	Battery back-up for IP encryption keys
Environmental	**Temperature:** **Air cooled option (AC0)** Operating Temperature 0° to +55°C **Air cooled Extended Range (ACE)** Operating Temperature 0° to +55°C **Air cooled industrial option (AC1)** Operating Temperature -20° to +55°C **Conduction cooled option (CC1)** Operating Temperature -40° to 71°C **EMC:** FCC 47CFR Part 2 EN55022 Equipment Class B

Ordering Codes

ADM-XRC-6TGE/z-y(m)(c)(a)(p)(e)(g)(t)

Virtex-6 device	z	LX240T, LX365T, LX550T, SX315T, SX475T
Virtex-6 speed	y	1, 2, 3
Memory Size Fitted	m	blank = 256MBytes per bank - 1GBytes for the board, /2 = 512MBytes per bank - 2GBytes for the board, /4 = 1024MBytes per bank - 4GBytes for the board
Cooling	c	blank = air cooled commercial, /ACE = air cooled Extended, /AC1 = air cooled industrial, /CC0 = conduction cooled Commercial, /CCE = conduction cooled Extended, /CC1 = conduction cooled industrial
Conformal Coating	a	blank = No coating, A = Acrylic (Humiseal 1B31), P = Polyurethane (Arathane 5750)
Pn4 Fitted	p	blank = not fitted, /P = Pn4 Connector fitted
Replace Ethernet link on Pn6 with x4 MGT link	e	blank = 10/100/1000Base-T Ethernet link - x4 MGT on Pn6, /M = No Ethernet Link - x8 MGT link on Pn6
Replace Ref Clk 1 on Pn6 with 2 GPIO	g	blank = MGT clock input on Pn6 - 44 GPIO on Pn6, /G = no MGT clock input on Pn6 - 46 GPIO on Pn6
XMC Connector Type	t	blank = XMC (VITA 42) Connectors , /X2 = XMC2 (VITA 61) Connectors
Note	#	not all FPGA speed grades available in all configurations. Contact Alpha Data for full details.

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