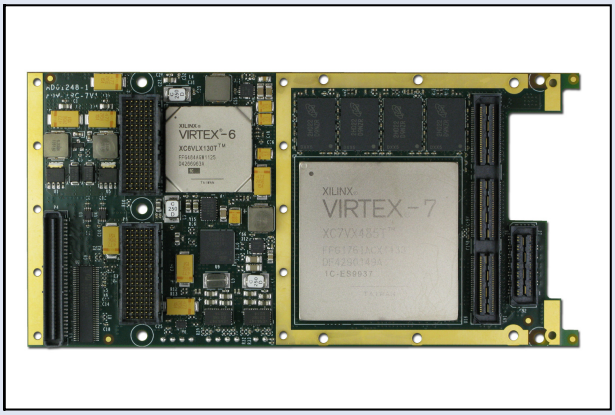
ADM-XRC-7V1

13th July 2016 **Datasheet Revision: 1.3**



Summary

The **ADM-XRC-7V1** is a high performance reconfigurable XMC (compliant to VITA Standard 42.0 and 42.3) based on the Xilinx Virtex-7 range of Platform FPGAs.
Features include PCI Express Gen2 interface, external memory, high density I/O, system monitoring and flash boot facilities.

A comprehensive cross platform API with support for **Microsoft Windows**, **Linux** and **VxWorks** provides access to the full functionality of these hardware features.
Placing the PCI Express bridge in bypass allows the creation of a Gen 2 x8 PCI Express endpoint design directly into the target FPGA. Target FPGAs VX330T and VX690T can also support Gen3 x8 PCI Express designs.
The optional fitting of the Pn4 connector provides an additional 64 General Purpose IO (GPIO) links to the carrier card.

The **ADM-XRC-7V1** is available in a cost reduced form for high-volume production orders (the build option removes the Virtex-6 Bridge device).

Features

Applications

Radar/Sonar Beamforming
ELINT
Image/Video Processing
Digital Signal Processing
Data Encryption

Target Device(s):

Xilinx Virtex-7: XC7V585T,XC7VX330T,XC7VX485T,XC7VX690T (FF(G)1761

Memory:

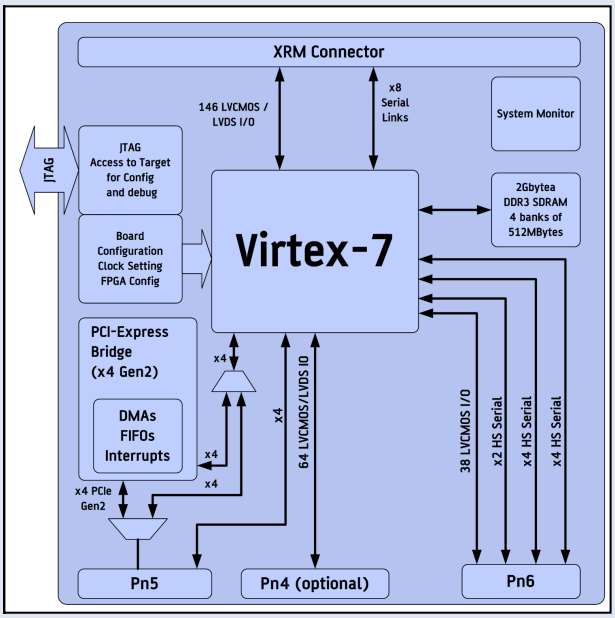
SDRAM - 2GByte in 4 independent banks (512MBytes/bank) of DDR3 SDRAM @ DDR-1600.
Alternatively, 4Gbit devices can be fitted giving 4GByte on board in 4 banks of 1GByte
or 8Gbit devices can be fitted giving 8GByte on board in 4 banks of 2GByte
FLASH - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.

Front I/O:

Up to 146 LVCMOS/LVDS I/O (programmable to 1.2, 1.5 or 1.8V)
8 High-Speed Serial Links

Rear I/O:

Up to 10 High-Speed Serial Links via Pn6 connector
38 LVCMOS 3.3V GPIO connections via Pn6 connector (VITA 46.9 X8d+X12d+X38s compatible pinout)
64 LVCMOS/LVDS GPIO connections via optional PMC Pn4 connector (1.8V levels with 2.5V compatible inputs)



Specification	
Product Name	**ADM-XRC-7V1**
Target Device(s)	Xilinx Virtex-7 XC7V585T,XC7VX330T,XC7VX485T,XC7VX690T (FF(G)1761
Interface	PCI Express Gen2 x1, x2 or x4 link to separate bridge device with 2GB/s local link to user FPGA 4 DMA Controllers Interrupt Controller
Memory	**SDRAM** - 2GByte in 4 independent banks (512MBytes/bank) of DDR3 SDRAM @ DDR-1600. Alternatively, 4Gbit devices can be fitted giving 4GByte on board in 4 banks of 1GByte or 8Gbit devices can be fitted giving 8GByte on board in 4 banks of 2GByte **FLASH** - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.
Front I/O	Up to 146 LVCMOS/LVDS I/O (programmable to 1.2, 1.5 or 1.8V) 8 High-Speed Serial Links
Rear I/O	Up to 10 High-Speed Serial Links via Pn6 connector 38 LVCMOS 3.3V GPIO connections via Pn6 connector (VITA 46.9 X8d+X12d+X38s compatible pinout) 64 LVCMOS/LVDS GPIO connections via optional PMC Pn4 connector (1.8V levels with 2.5V compatible inputs)
Clocks	Low-jitter 250MHz reference clock, suitable for SerDes applications Low-jitter 200MHz reference clock for IOB delay circuits Custom clock inputs available through the XRM interface Two Software-Programmable Clocks
Device Configuration	PCI Express direct to SelectMAP port From Flash direct on power up External JTAG connector
Software	Drivers for Microsoft Windows, Linux and VxWorks The ADM-XRC Gen3 SDK provides the example C and HDL source code, giving software engineers and FPGA designers a head start in creating applications.
Environmental	**Temperature:** **Air cooled option (AC0)**: Operating Temperature 0° to +55°C **Air cooled extended (ACE)**: Operating Temperature 0° to +70°C **Air cooled industrial option (AC1)**: Operating Temperature -40° to +70°C **Conduction cooled option (CC0)**: Operating Temperature 0° to 55°C **Conduction cooled extended (CCE)**: Operating Temperature 0° to 70°C **Conduction cooled industrial option (CC1)**: Operating Temperature -40° to 70°C **Conformal Coating:** Acrylic (Humiseal 1B31) Polyurethane (Arathane 5750) **EMC:** FCC 47CFR Part 2 EN55022 Equipment Class B **RoHS Compliance:** All standard products are RoHS compliant. Please contact Alpha Data Sales for details of Tin/Lead build options.

Ordering Code		
ADM-XRC-7V1/z-y(m)(c)(a)(p)(t)		
Virtex-7 device	z	V585T=XC7V585T, VX330T=XC7VX330T, VX485T=XC7VX485T,VX690T=XC7VX690T
Virtex-7 speed	y	1, 2, 3
Memory	m	blank = 2GBytes on board SDRAM (Four banks of 512MBytes), /4 = 4GByte on board SDRAM (Four banks of 1GByte), /s8 = 8GByte on board SDRAM (Four banks of 2GByte)
Cooling	c	blank = air cooled commercial, /ACE = air cooled Extended, /AC1 = air cooled industrial, /CC0 = conduction cooled Commercial, /CCE = conduction cooled Extended, /CC1 = conduction cooled industrial
Conformal Coating	a	blank = No coating, A = Acrylic (Humiseal 1B31), P = Polyurethane (Arathane 5750)
Pn4 Fitted	p	blank = not fitted, /Pn4 = Pn4 Connector fitted
XMC Connector Type	t	blank = XMC (VITA 42) Connectors , /X2 = XMC2 (VITA 61) Connectors
Note		not all FPGA speed grades available in all configurations. Contact Alpha Data for full details.

Address: 4 West Silvermills Lane,
Edinburgh, EH3 5BD, UK
Telephone: +44 131 558 2600
Fax: +44 131 558 2700
email: sales@alpha-data.com
website: http://www.alpha-data.com

Address: 3507 Ringsby Court Suite 105,
Denver, CO 80216
Telephone: (303) 954 8768
Fax: (866) 820 9956 toll free
email: sales@alpha-data.com
website: http://www.alpha-data.com