Implementing a DDR4 SDRAM Interface in the ADM-VA600

Alpha Data Parallel Systems Ltd.

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1 Introduction

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The ADM-VA600 is a Space VPX (VITA 78) reconfigurable computing card featuring a AMD Versal XCVC1902 Adaptive SoC and two banks of 72-bit wide DDR4 SDRAM that can operate at up to 2133 GT/s. This document provides guidelines on implementing a DDR4 SDRAM interface in the ADM-VA600 using the memory controllers in the Network-on-Chip (NoC) infrastructure of a Versal Adaptive SoC.

Configuration of the Network-on-Chip memory controllers depends upon selecting the correct board part for a Vivado project, and an ADM-VA600 board file is required. For information about ADM-VA600 board files, see AD-AN-0142, “ADM-VA600 Board File”. Table 1 below lists ADM-VA600 order codes and their memory configurations.

Order code prefix	Banks x Bank capacity	Bank timing (CL-nRCD-nRP)	Memory part
ADM-VA600/DEV	2 x 8 GiB	JEDEC DDR4-2133P (15-15-15)	Teledyne DDR4T08G72AZR1A

Table 1: ADM-VA600 memory configurations by order code

The physical width of each memory bank is 72 bits, meaning that 8 bits of a physical memory word are an ECC (Error Correction Code) with the other 64 bits used for data.

1.1 DDR4 SDRAM-related I/O bank assignments in the ADM-VA600

Figure 1 shows the I/O banks of the VC1902 Adaptive SoC and highlights the banks used for DDR4 SDRAM interfaces in the ADM-VA600.

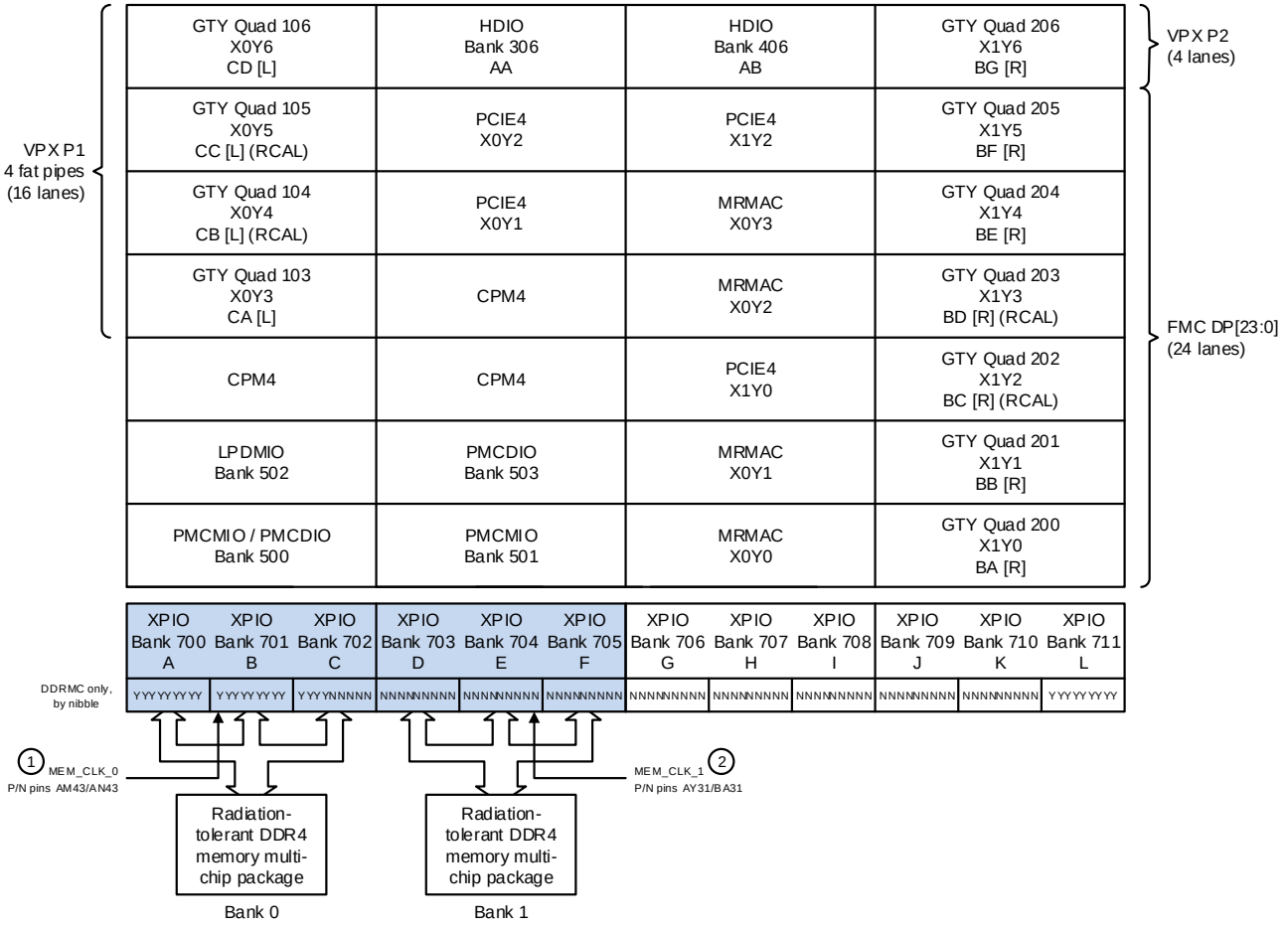


Figure 1: I/O banks in VC1902 Adaptive SoC (VSVA2197 package)

With reference to Figure 1 above, the following board features are highlighted:

1. The reference clock for DDR4 SDRAM bank 0's memory controller is `MEM_CLK_0`. For `PACKAGE_PIN` and other constraints, see Section 4.
2. The reference clock for DDR4 SDRAM bank 1's memory controller is `MEM_CLK_1`. For `PACKAGE_PIN` and other constraints, see Section 4.

2 Using the NoC memory controllers

Instantiating the AXI Network-on-Chip IP in a Vivado Block Diagram design is straightforward. Figure 2 shows a simple design that connects the one and only CIPS (Control and Processing System) IP instance to two banks of DDR4 SDRAM, with one AXI NoC IP instance per bank:

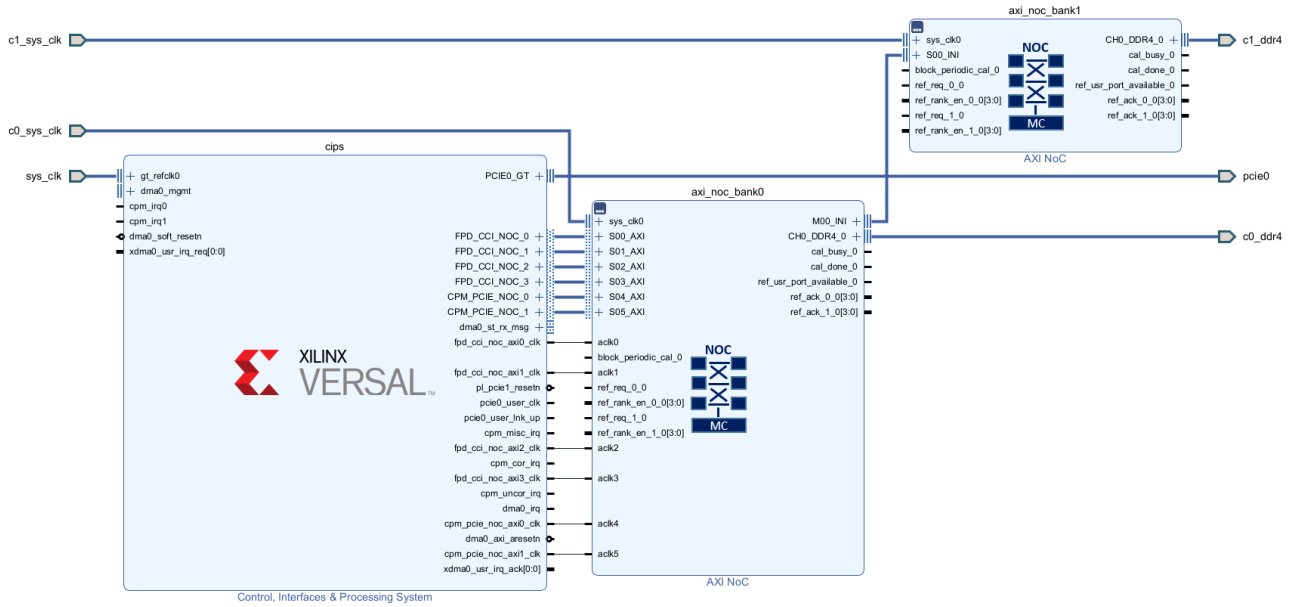


Figure 2: Simple Block Diagram design using NoC DDR4 SDRAM contollers

In the above example, the interfaces of the CIPS IP that are enabled allow shared access to the DDR4 SDRAM by either (i) the CPM PCIe block or (ii) the ARM CPU cores in the Processing System (PS). However, a discussion of how to configure the CIPS IP is outside the scope of this document; please refer to AMD PG352 for details.

There is no visible reset signal in Figure 2 for either AXI NoC IP instance. This is because in a Versal Adaptive SoC, the only way to reset the Network-on-Chip and DDR4 SDRAM controllers is via registers in the Platform Management Controller (PMC) component of the CIPS.

Figure 3 below shows another example Vivado Block Diagram design, this time with a single AXI NoC IP instance controlling both DDR4 SDRAM banks in an interleaved manner. The choice of interleaved vs. non-interleaved is made in the configuration GUI for the AXI NoC IP; see Section 3.1 for details.

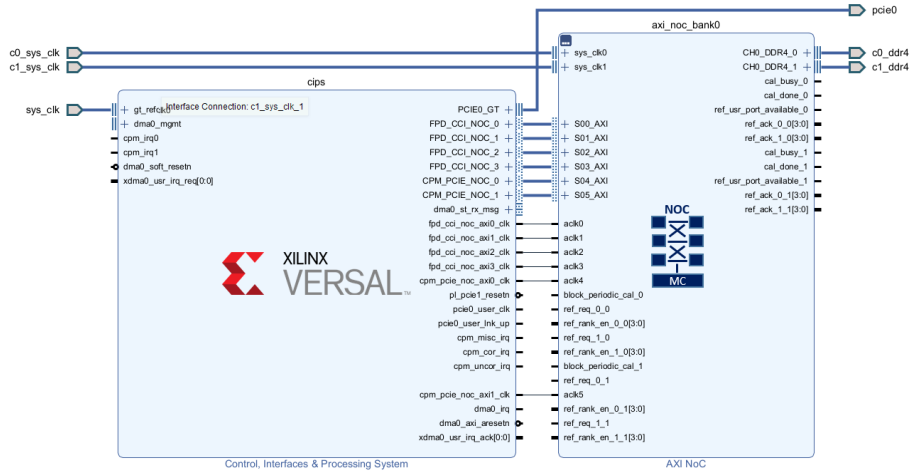


Figure 3: Simple Block Diagram design using NoC DDR4 SDRAM contollers with Interleaving

3 How to configure the NoC memory controllers

This section contains information about configuring the Network-on-Chip memory controllers for the ADM-VA600's two banks of DDR4 SDRAM. It is assumed that the reader has AMD PG313 to hand; only information

pertaining specfically to using the AXI Network-on-Chip IP with the ADM-VA600 is covered in this section.

Information valid for Vivado 2022.1 or later

Screen captures depicting how to set various configuration options are obtained from the AXI Network-on-Chip IP configuration GUI. The information concerning the AXI Network-on-Chip IP in this document applies to Vivado 2022.1 or later.

ADM-VA600 board part required for Vivado project

It is assumed, throughout this section and following subsections, that one of the ADM-VA600 board parts is in use for the Vivado project. If a Vivado project does not use the correct board part, the board interfaces defined by the board file will not be available for selection in the AXI NoC IP configuration GUI. ADM-VA600 board files are covered in AD-AN-0142, “ADM-VA600 Board File”.

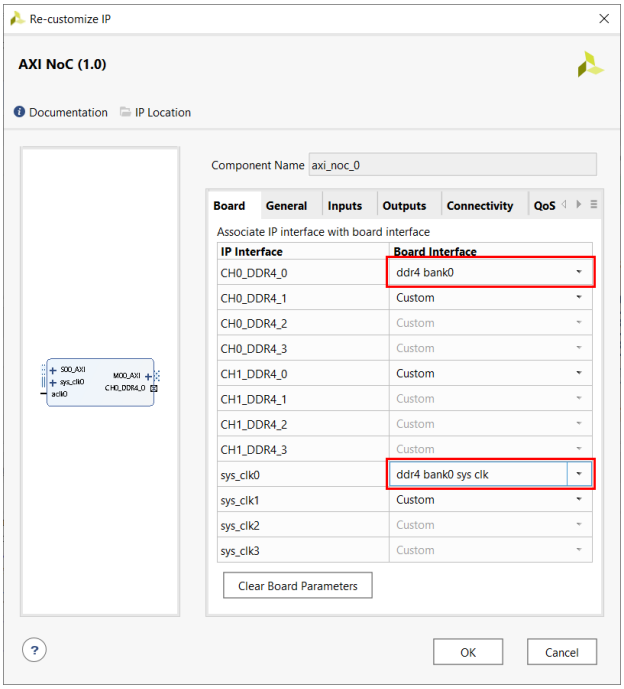
3.1 Board tab

On the “Board” tab, the designer must decide whether to use the DDR4 SDRAM controller in (a) non-interleaved or (b) interleaved mode.

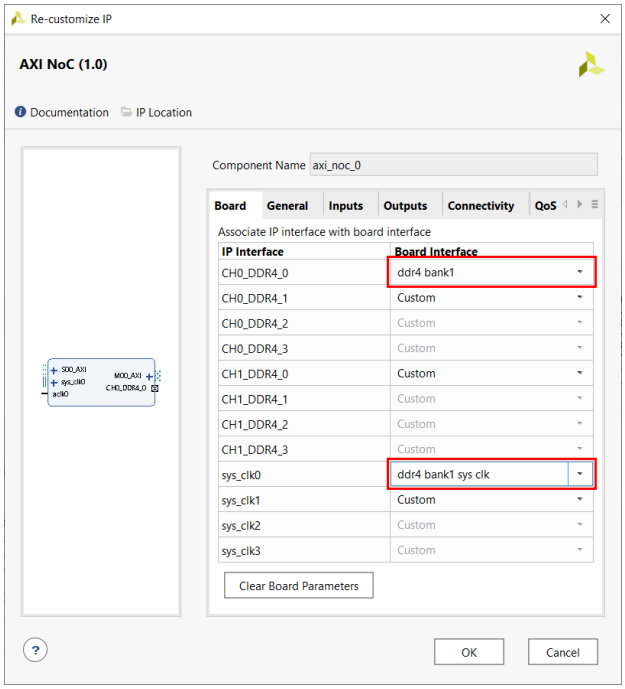
(a) ***Non-interleaved*** – The AXI NoC IP instance controls a single bank of DDR4 SDRAM. This choice is illustrated in Figure 4 below.

NOTE: If the application is to make use of both banks of DDR4 SDRAM without interleaving, another AXI NoC IP instance must be instantiated as shown in Figure 2.

(b) ***Interleaved*** – The AXI NoC IP instance controls both banks of DDR4 SDRAM and interleaves data across them, as shown in Figure 3. This effectively doubles DDR4 SDRAM bandwidth provided that AXI transactions to and from the memory controllers utilize sufficiently long bursts. This choice is illustrated in Figure 5 below.



(a) Using DDR4 SDRAM bank 0



(b) Using DDR4 SDRAM bank 1

Figure 4: Configuring AXI NoC IP to use a single bank of DDR4 SDRAM

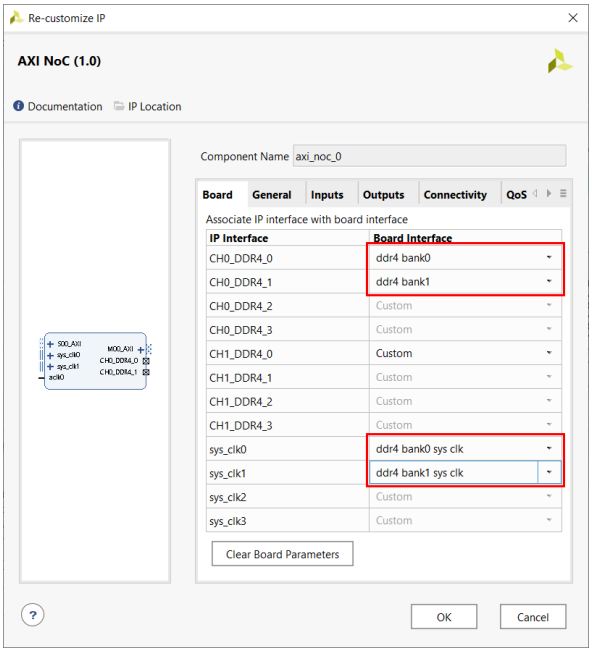


Figure 5: Configuring AXI NoC IP to use both banks of DDR4 SDRAM in interleaved mode

3.2 General tab

On the “General” tab, the ***Memory Controller*** setting must be consistent with the board interface choices made on the ***Board*** tab:

(a) ***Non-interleaved*** – Set ***Memory Controller*** to ***Single Memory Controller*** if the AXI NoC IP instance is to control a single bank of DDR4 SDRAM, consistent with the board interface settings shown in Figure 4 above.

(b) ***Interleaved*** – Set ***Memory Controller*** to ***x2 Interleaved Memory Controllers*** if the AXI NoC IP instance is to control both banks of DDR4 SDRAM in interleaved mode, consistent with the board interface settings shown in Figure 5 above.

Figure 6 below shows the the ***Memory Controller*** setting on the “General tab”:

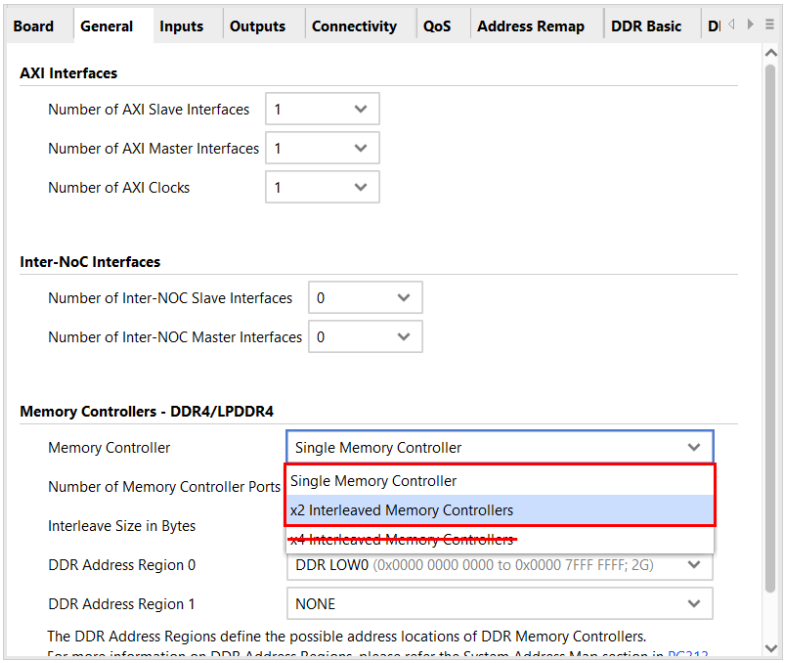


Figure 6: ***Memory Controller*** setting on AXI NoC IP ***General*** tab

The rest of the “General” tab may be set according to application requirements.

3.3 Inputs, Outputs, Connectivity & QoS tabs

The options on the “Inputs”, “Outputs”, “Connectivity” & “QoS” tabs are at the discretion of the designer. Please refer to AMD PG313 for information about these options.

3.4 DDR Basic tab

When DDR4 SDRAM board interface(s) are selected in the “Board” tab (see Section 3.1), the appropriate IP presets defined by the board file are applied to the AXI NoC IP instance. As a result, most of the settings in the “DDR Basic” tab become inoperable (grayed out). Settings that remain operable may be tweaked by the designer.

Alpha Data recommends leaving ***System Clock*** set to ***Differential*** and making use of the dedicated DDR4 SDRAM controller reference clocks (`MEM_CLK_0` & `MEM_CLK_1` – see Figure 1) as shown in Figure 4 and Figure 5. Use of other clocks as DDR4 SDRAM controller reference clocks may permit reliable DDR4 SDRAM operation but is not tested by Alpha Data.

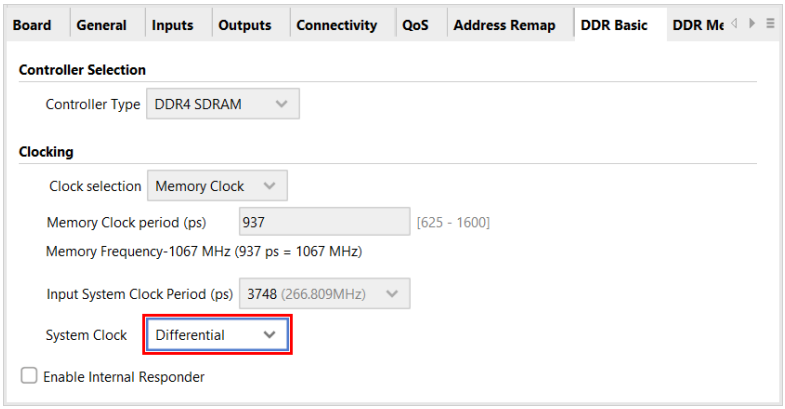


Figure 7: AXI NoC IP “DDR Basic” tab

Enable Internal Responder may be set according to application requirements.

3.5 DDR Memory tab

On the “DDR Memory” tab, the settings under ***Timing Parameters*** and ***Mode Register Settings*** can be tweaked if desired. These are set according to the JEDEC timing that is applied by the board file (e.g. DDR4-2133P), but can be tweaked by the designer. The standard JEDEC timing should be sufficient for reliable DDR4 SDRAM operation, however.

Because ECC is in use and prevents use of masked writes, ***Write DBI*** should be set to ***NO DM DC DBI*** in order to reduce runtime power consumption. Likewise, the ***Read DBI*** checkbox should be checked (enabled) in order to further reduce runtime power consumption.

CAS Latency nCK and/or ***CAS Write Latency nCK*** may be tweaked by the designer, but Alpha Data recommends leaving them at their default values for best performance.

The rest of the settings on the “DDR Memory” tab should be left unchanged from defaults.

Figure 8 below shows the settings that may be tweaked by the designer highlighted by blue boxes:

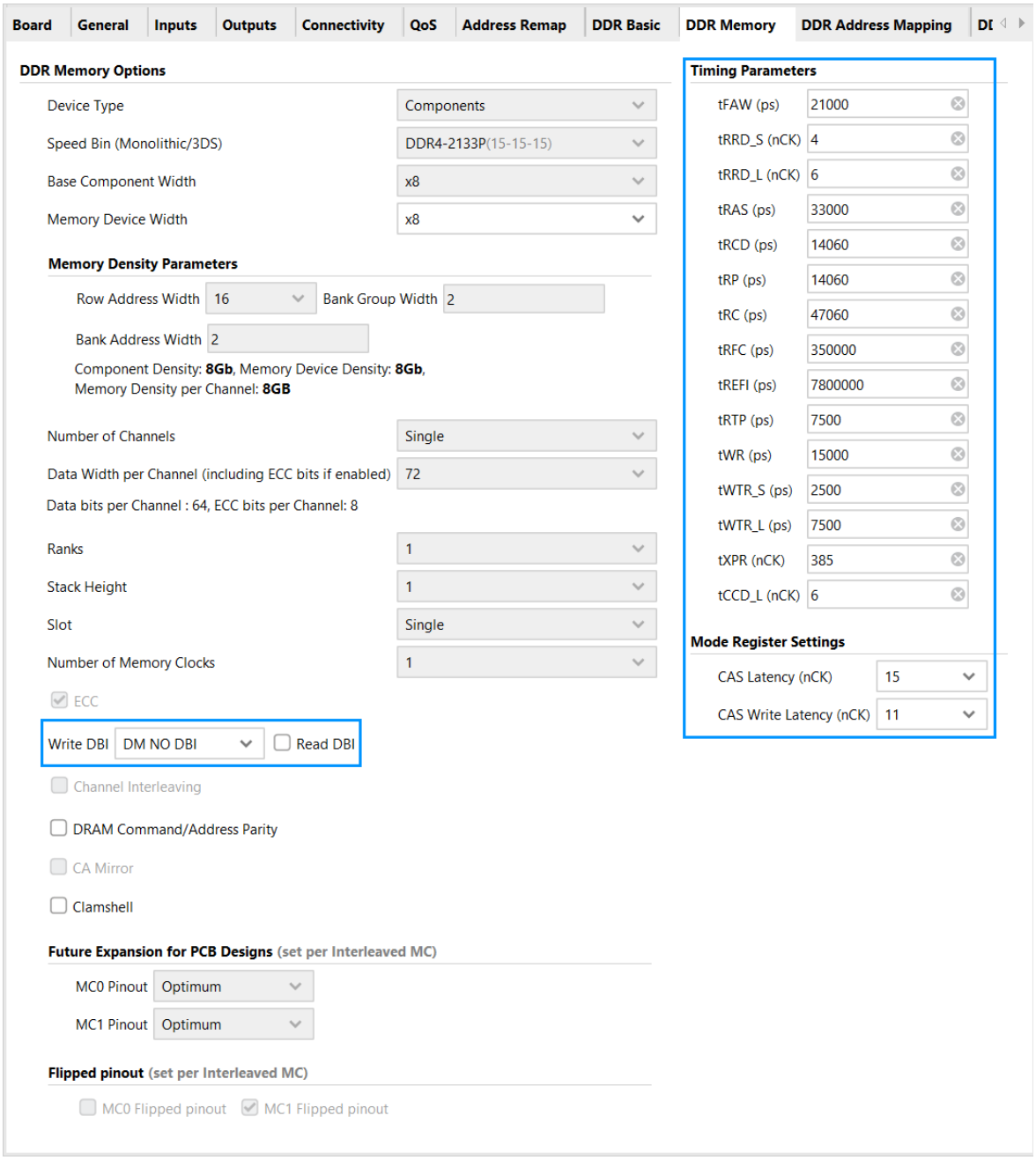


Figure 8: Settings that may be tweaked on AXI NoC IP “DDR Memory” tab

3.6 DDR Address Mapping

The options on the “DDR Address Mapping” tab can be set according to application requirements. Please refer to AMD PG313 for information about these options.

3.7 DDR Advanced tab

Alpha Data recommends leaving ***Initialize memory for ECC*** enabled for most applications, which means that the memory controller establishes good ECC in every physical memory word after completing calibration.

Establishing good ECC when *Initializate memory for ECC* is disabled

If ***Initialize memory for ECC*** is disabled, it is the responsibility of the designer to ensure that something (an APU / RPU application or user-defined logic) establishes good ECC values in every physical memory word during application initialization.

Failure to establish good ECC before attempting to read from DDR4 SDRAM results in an ECC error. An ECC error may generate an exception if the read originates from a CPU core.

ECC Initialization Size (MB) should generally be left at the default value so that good ECC values are established for the entire memory bank.

The other options on the “DDR Advanced” tab can be set according to application requirements. Please refer to AMD PG313 for information about these options.

4 PACKAGE_PIN and other constraints

For ready-to-use constraints files covering all DDR4 SDRAM-related pins, see “ADM-VA600 Standalone DDR4 Test FPGA Design” in the ADM-VA600 PL Examples.

4.1 DDR4 SDRAM top-level ports

The board file defines the pinout for DDR4 SDRAM board interfaces, and so constraints files containing `PACKAGE_PIN` constraints are **not** required.

Constraints such as `IOSTANDARD` etc. are **not** required because they are supplied by the AXI NoC IP.

However, the default `SLEW` value of `FAST` must be overridden for certain top-level DDR4 SDRAM ports using a constraints file. The following constraints must be present in any design for the ADM-VA600 that uses either or both DDR4 SDRAM banks:

```
set_property SLEW MEDIUM [get_ports {c?_ddr4_act_n*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_adr*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_ba*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_bg*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_ck_*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_cke*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_cs_n*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_odt*}]
```

The above constraints assume that the top-level ports for DDR4 SDRAM interfaces are prefixed by either `c0` or `c1`. If this is not true for your design, the above constraints must be modified accordingly to use the appropriate prefix.

In summary, the only constraints file (`.xdc` file extension) required for the DDR4 SDRAM top-level ports is one that overrides `SLEW` as shown above. For an example, see the file `ddr4sdram_slew.xdc` from “ADM-VA600 Standalone DDR4 Test FPGA Design” in the ADM-VA600 PL Examples.

4.2 DDR4 SDRAM controller reference clocks

`PACKAGE_PIN` and `DIFF_TERM` constraints are **not** required for the top-level ports corresponding to the DDR4 SDRAM controller reference clocks because the board file provides the required information. Likewise, `IOSTANDARD` constraints are **not** required because the AXI NoC IP provides them.

Clocks should not be defined (using `create_clock`) for the DDR4 SDRAM controller reference clocks because the AXI NoC IP automatically defines a clock according to the ***Input System Clock Period (ps)*** value from the configuration GUI (see Figure 7). This value is provided by IP presets defined by the board file.

In summary, no constraints files (`.xdc` file extension) are required for the DDR4 SDRAM controller reference clocks.

5 Known issues

5.1 Incorrect MR5 value when simulating certain AXI NoC IP configurations

Vivado versions affected

The following issue is known to apply to Vivado 2022.1 to 2023.2 inclusive.

If the AXI NoC IP is simulated as part of a Unit Under Test (UUT), and it is configured such that "Enable Internal Responder" is disabled (unchecked) as in Figure 7, then any testbench for the UUT must provide models of DDR4 SDRAM chips that respond appropriately to the c***N***_ddr4_* signals driven by the UUT.

If, additionally, the AXI NoC IP is configured to use DBI for reads and/or writes (Section 3.5), then the following issue arises:

- The behavioral model of the AXI NoC IP writes the same Mode Register 5 (MR5) value of 14'b00010000000000 into the DDR4 SDRAM chip models regardless of the DBI-related IP settings. This means the DDR4 SDRAM chip models consider DBI to be disabled in all cases.
- On the other hand, the behavioral model of the AXI NoC IP appears to honour the DBI-related IP settings when driving the c***N***_ddr4_dq and c***N***_ddr4_dm_dbi_n signals.
- The result is that the AXI NoC IP behaves inconsistently with respect to the DDR4 SDRAM chip models and the simulation produces incorrect results if any reads or writes of DDR4 SDRAM memory locations are attempted.

The only known workaround at present is, before launching a simulation, to configure the AXI NoC IP to disable DBI for both reads and writes. This can be done by pasting the following into Vivado's Tcl console when the Block Diagram containing the AXI NoC IP is open:

```
set_property -dict [list \
  CONFIG.MC_READ_DBI {false} \
  CONFIG.MC_WRITE_DM_DBI {DM_NO_DBI} \
] [get_bd_cells <your NoC BD cell name>]
validate_bd_design
save_bd_design
```

Alternatively, disabling DBI for both reads and writes can be done via the "DDR Memory" tab of the AXI NoC IP configuration GUI (see Section 3.5).

Use of DBI recommended when running in hardware

For synthesis and implementation, Alpha Data recommends enabling DBI for reads and writes in order to reduce runtime power consumption.

6 Related documents

1. PG313 – LogiCORE IP Product Guide "Versal Adaptive SoC Programmable Network on Chip and Integrated Memory Controller", AMD Inc. (formerly Xilinx Inc.)
2. PG352 – LogiCORE IP Product Guide "Control Interfaces and Processing System", AMD Inc. (formerly Xilinx Inc.)

3. UG863 – User Guide “Versal Adaptive SoC PCB Design”, AMD Inc. (formerly Xilinx Inc.)
4. DS 60S 219460 – Data Sheet “4GB / 8GB Radiation Tolerant DDR4 Memory”, Teledyne Imaging
5. AD-UG-1456 – ADM-VA600 User Manual, Alpha Data Parallel Systems Ltd.
6. AD-AN-0142 – Application note “ADM-VA600 Board File”, Alpha Data Parallel Systems Ltd.
7. AD-UG-0183 – User Guide “ADM-VA600 Standalone DDR4 Test FPGA Design”, Alpha Data Parallel Systems Ltd.

Document version history

Document version	Notes
1.0	Initial version.

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