ADPe-XRC-4

Hardware Manual

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Revision History

Revision	Date	Comments
0.1	Jun-06	Initial
0.2	Jan-07	
0.2+	Feb-07	
	June-07	Cooling and removal of fans from heatsinks

Contents

1 Introduction

The ADPe-XRC-4 is an advanced PCIe card supporting Xilinx Virtex-4 FX™ (V4FX) devices, the latest development in FPGA technology. The ADPe-XRC-4 supports V4FX100, or V4FX140 devices with two embedded PowerPC processors.

The ADPe-XRC-4 utilises an FPGA PCIe bridge developed by Alpha Data supporting 4 lane PCI express. A high speed multiplexed address and data bus connects the bridge to the target FPGA. Future versions of the bridge will support upto 8 Lane PCIe

Memory resources provided on-board include DDR2 SDRAM, DDR2 SSRAM and flash, all of which are optimised for direct use by the FPGA using IP and toolkits provided by Xilinx.

Flexible I/O is the key to the ADM-XRC-II series of boards and the ADPe-XRC-4 is compatible with a wide selection of XRM modules which use the 180 pin Samtec interface.

1.1 Specifications

The ADPe-XRC-4 supports high performance PCI-express operation without the need to integrate proprietary cores into the FPGA.

- Physically conformant to PCIe * 8 lane slot
- High performance PCIe and asynchronous local bus
- Local bus speeds of up to 80MHz
- One bank of 256K * 32 bits of DDR2 SSRAM – option for 512K * 32 bits
- Four independent banks of DDR2 SDRAM supporting upto 1Gbytes
- 32MB Flash
- User clock programmable between 5MHz and 200MHz
- User front panel adapter with up to 146 free IO signals
- On board 125MHz LVPECL oscillator
- 8 x RocketIO Multi-Gigabit Transceiver Connections (optional) @ 2.5Gb/s

2 Installation

This chapter explains how to install the ADPE-XRC-4 onto a PC motherboard.

2.1 Motherboard requirements

The ADPe-XRC-4 should be installed in an 8 or 16 lane PCI express slot. It may be possible to fit the card into *1 and *4 slots by use of a suitable adapter. Ensure that the motherboard satisfies this requirement before powering it up

2.2 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.

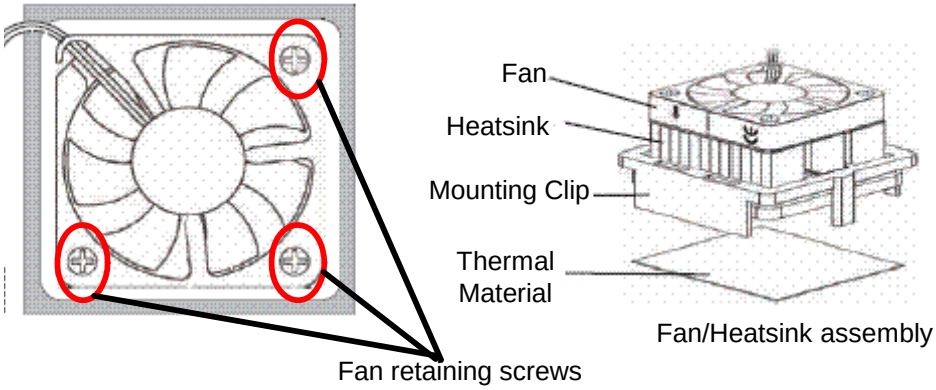
Avoid flexing the board.

2.3 Cooling

Memory-intensive applications can dissipate significant amounts of power in the FPGA. Users running such applications on the ADPe-XRC-4 should ensure that an adequate flow of air is maintained over the heatsinks and chip coolers.

The ADPe-XRC-4 card is supplied with heatsinks and integral fans attached to both target and bridge FPGA devices. In systems which have a single slot height restriction the fans may be removed from the heatsinks providing adequate air flow can be maintained across the ADPe-XRC-4 card within the system.

The fan can be removed from the by unscrewing the 3 retaining screws which secure the fans to the heatsink as below :-



3 Hardware Overview

The ADPe-XRC-4 is based on the architecture of the ADM-XRC and ADP-XPI cards with changes to accommodate the enhanced resources and needs of the Virtex 4 FX devices and interfacing to the PCI Express host bus

It follows the architecture of the ADM-XRC series and decouples the “target” FPGA from the “bridge” device to allow the entire target to be available for user applications. This ensures the user can be up and running with the minimum of effort and without the complexity of a PCI express design.

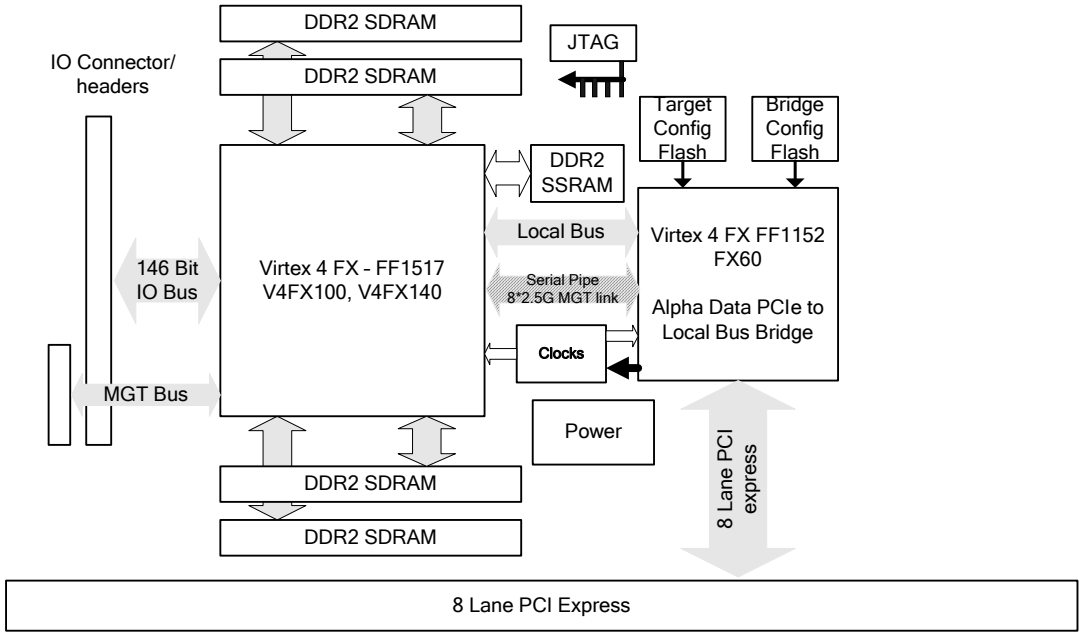
The bridge includes local bus control and monitoring together with flexible configuration options for the bridge and the target device.

The bridge is capable of 4 lane PCI express operation reverting back to 1 lane operation as required by the host. The local bus supports 64-bit operation at up to 80MHz

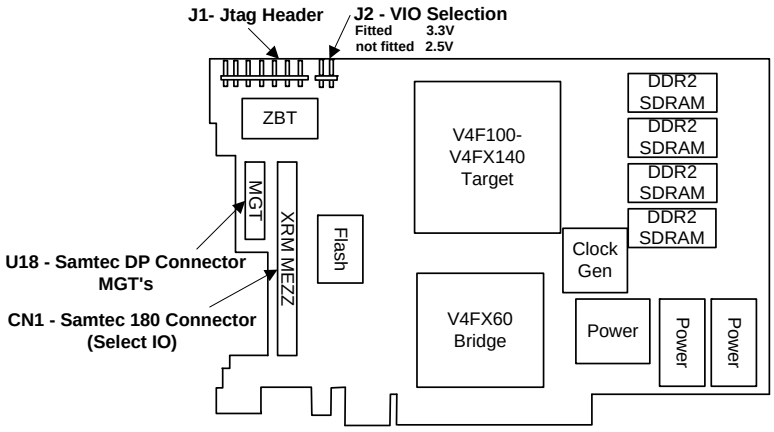
The target FPGA is a Virtex-4 FX device incorporating FPGA fabric, multi-gigabit transceivers and two PowerPC cores.

DDR2 SDRAM, DDR2 SSRAM and flash memory connect to the target FPGA and are supported by Xilinx or third party IP.

IO functionality is provided using XRM modules connecting to the 180 pin SAMTEC QSE and 28 pin SAMTEC QSE DP connectors.



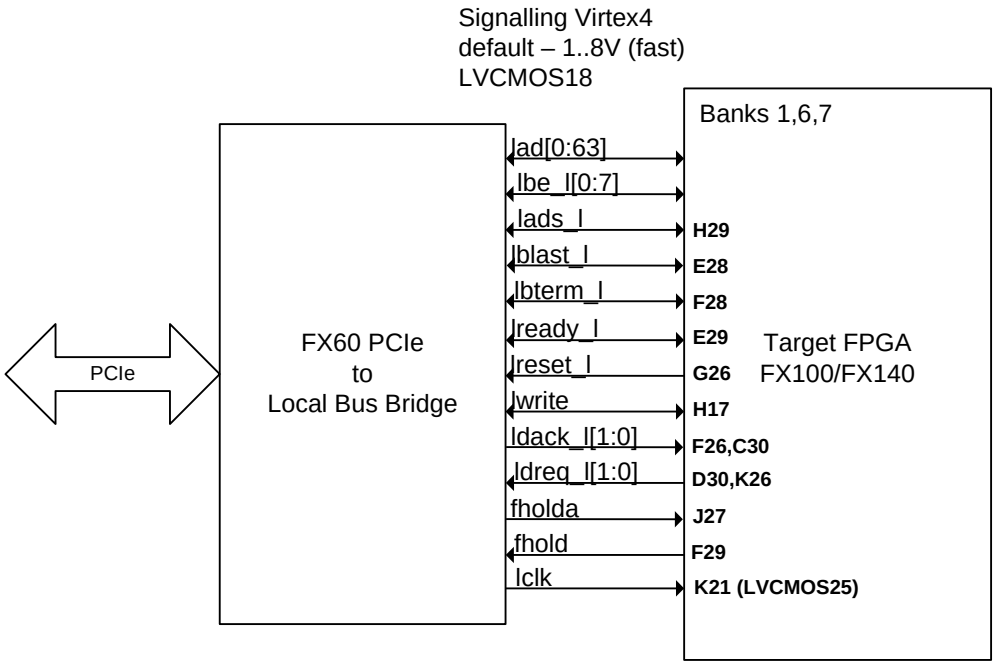
The physical layout is shown in the diagram below.



4 Local Bus Architecture

The ADPE-XRC-4 implements a multi-master local bus between the bridge and the target FPGA using a 32 or 64 multiplexed address and data path. The bridge design is asynchronous and allows the local bus to be run faster or slower than the PCIe bus clock to suit the complexity of the user design.

4.1 Local Bus signals



Signal	Type	Purpose
Lad[0:63]	bidir	Address and data bus.
lreset_l	unidir	Reset to target
lads_l	bidir	Indicates address phase
lblast_l	bidir	Indicates last word
lbterm_l	bidir	Indicates ready and requests new address phase
lready_l	bidir	Indicates that target accepts or presents new data
Lclk	unidir	Clock to synchronise bridge and target
Lbe_l[0:7]	bidir	Byte qualifiers
dreq_l[0:1]	unidir	DMA request from target to bridge
dack_l[0:1]	unidir	DMA acknowledge from bridge to target
Fhold	unidir	Target bus request
Fholda	unidir	Bridge bus acknowledge

4.2 Local Bus Transfers

Please refer to the ADM-XRC SDK Help for Windows supplied with the ADPE-XRC-4 for information on local bus transfers.

5 Target FPGA

The target FPGA is a virtex 4 FX100 or FX140 in an FF1517 package. On the ADPE-XRC-4, all of the resources such as DDR, DDR2 SSRAM, IO and Flash are available no matter what device is fitted.

IO banks 9, 11 and 13 provide the User IO to the front panel . The VCCIO voltage for banks 9, 11 and 13 is selectable using J2.

J2 Link Posn	VCCIO – Front IO
Fitted	+3V3
Not fitted	+2V5

5.1 Configuration

The target FPGA can be configured using two primary mechanisms. In the first, JTAG from the J6 header can be used to perform downloading of bit-streams as well as remote debug using tools such as GDB and ChipScope / Pro. The drawback of using JTAG is that a download cable must be connected to the board.

The ADPE-XRC-4 provides a SelectMAP port between the bridge and the target device mapped to the PCI bus. This enables very rapid download of configuration data controlled by driver and API code in the host. The maximum speed that can be achieved is 80 Mbytes per second.

5.2 Clocks

The ADPe-XRC-4 provides numerous clock sources detailed below

5.2.1 LCLK

The Local Bus can be used at up to 80 MHz and all timing is synchronised to LCLK between the Bridge and User FPGAs. The LCLK frequency is set by writing to the board control logic. (See SDK for details and example application).
Note: If the user FPGA application includes a DCM driven by LCLK (or one of the other programmable clocks), the clock frequency should be set prior to FPGA configuration.

5.2.2 MCLK

This a general purpose user clock available to the Target FX100/FX140 through a global clock input. The MCLK frequency is set by writing to the board control logic and is programmed in the same manner as LCLK.
(See SDK for details and example application).

5.2.3 REFCLK

In order to make use of the IDELAY features of Virtex™-4, a stable low-jitter clock source is required to provide the base timing for tap delay lines in each IOB in the User FPGA. The ADPe-XRC4 is fitted with a 200MHz LVPECL (LVDS optional) oscillator connected to global clock resource pins. This reference clock can also be used for application logic if required.

5.2.4 PCIe Reference Clock

A 100MHz PCIe reference clock input from the PCIeconnector is converted to 250MHz by an ICS874003-02. The 250MHz clock is then connected to one of the dedicated MGT clock inputs on the user FPGA.

5.2.5 User MGT Clock

The clock for the user MGT's which go to the front panel XRM module is supplied from a fixed reference oscillator. The default value of the frequency for this oscillator is 125MHz but other values can be fitted on request

5.2.6 XRM Global Clock Input

The XRM interface provides a differential input to the User FPGA global clocking resources.

5.2.7 XRM Regional Clocks

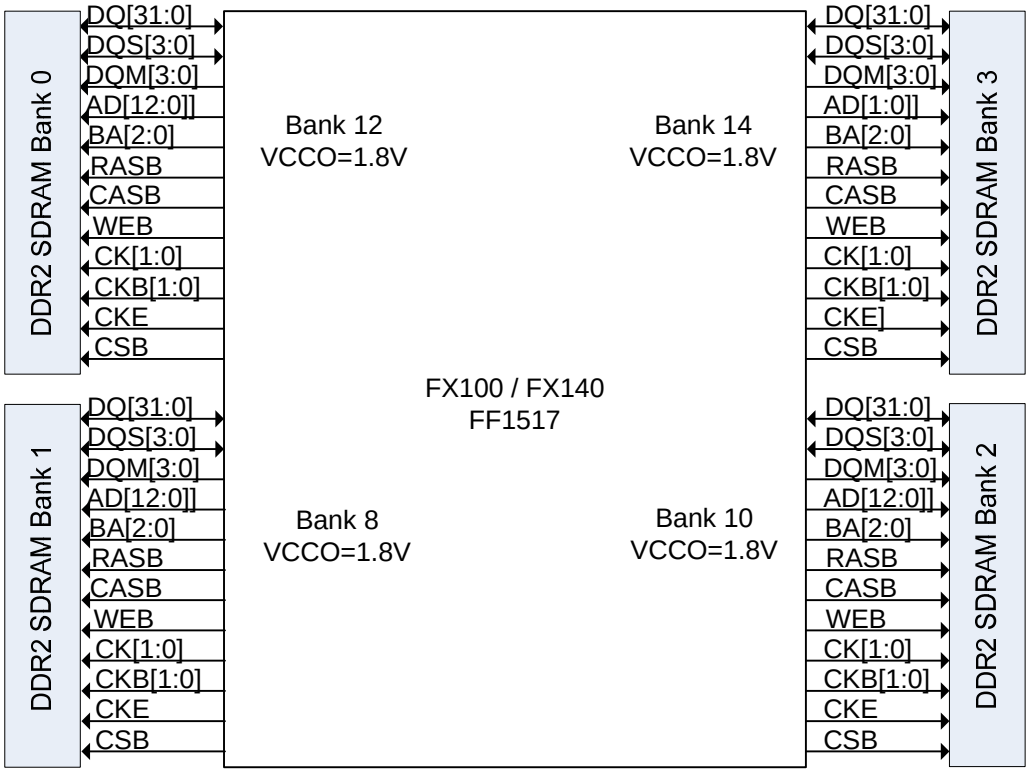
The XRM interface provides 8 clock lines that can be either be used single-ended or as 4 LVDS differential pairs. These clocks are routed to Clock-Capable inputs on the User FPGA, providing access to its regional clock capabilities.
Each clock pair can be coupled with 16 pairs of XRM bus signals, as shown in Table 1 below:

XRM Clocks	Clock Region	XRM bus pairs
0 & 1 (Pair 0)	X0Y6 / X0Y7	1 – 16
2 & 3 (Pair 1)	X0Y5 / X0Y6	17 – 32
4 & 5 (Pair 2)	X0Y3 / X0Y4	33 – 48
6 & 7 (Pair 3)	X0Y2 / X0Y3	49 – 64

Table 1 XRM Bus Regional Clocks

5.3 SDRAM DDR Memory

The ADPe-XRC-4 provides 4 independent banks of 32 bit DDR2 SDRAM. The devices fitted are MT47H6416HR-37E-R or equivalent.



The pins required for the SDRAM controller for each bank are listed below.

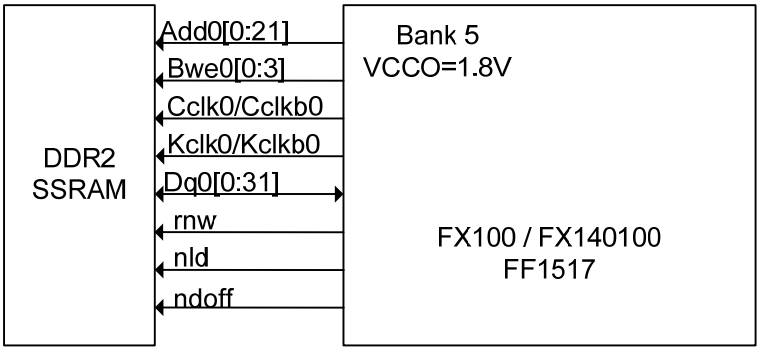
Name	Type
DDR_ad[0:12]	Output
DDR_dq[0:31]	Bidir
DDR_dqs[0:3]	Bidir
DDR_rasb	Output
DDR_casb	Output
DDR_web	Output
DDR_ba[0:1]	Output
DDR_clk	Output
DDR_clkb	Output
DDR_csb	Output
DDR_cke	Output
DDR_dm[0:1]	Output
DDR_clk_fb	Input

The DDR controller uses SSTL1 IOB's for data and control and SSTL1 for address and clocks - Please refer to the UCF for locations of the DDR2 pins.

The ADPe-XRC-4 is designed to support the Xilinx MIG DDR2 interface cores.

5.4 DDR2 SSRAM

The ADPe-XRC-4 supports one bank of CIO DDR2 SSRAM memory. The devices fitted are Samsung 1Mx36 (K7I323682M-FC16) parts or a functional equivalent. As an upgrade option 2Mx36 devices can also be fitted.



The pins required for the SSRAM controller bank are listed below.

Name	FPGA Pin Type	Description
ZBTx_ad[0:21]	Output	Address bus
ZBTx_dq[0:31]	Bidir	Data bus
ZBTx_rw	Output	Read(1) / Write(0)
ZBTx_bwe{0..3]	Output	Byte enables for writes
ZBTx_nld	Output	Initiates a transaction
ZBTx_Cclk/ZBTx_nCclk	Output	SSRAM Output Data Clock
ZBTx_Kclk/ZBTx_nKclk	Output	SSRAM Clock for Inputs
ZBTx_DOFF	Output	SSRAM DLL Enable

The SSRAM pins should be configured for HSTL_II_18 operation

The SSRAM clock Cclks and Kclks are intended to be used with clock-forwarding implemented in a DDR IOB with a DCM used to adjust for SSRAM clock to output delays on the data input path to the FPGA.

5.5 Power Supply

The PCIe connectors supply +12V and +3V3 to the ADPe-XRC-4 and both of these rails are used with the card.

6 Front Panel I/O

The ADPE-XRC-4 supports standard XRM's used on the ADM-XRC-II and ADP-XPL cards and also has an additional connector that brings 7 MGT channels upto the XRM Module site using a differential 28 pin Samtec QSE-DP series connector to maintain signal integrity.

The ADPE-XRC-4 supports the standard Samtec 180 pin connector but using either with 2.5V or 3.3V signalling which is globally selected using JP1

J2 Link Posn	VCCIO – Front IO
Link present	+3V3
Link not present	+2V5

6.1 XRM Interface – Standard Signals and Power

The XRM interface is implemented on CN1, a 180 pin Samtec connector type QSH, with the pin-out as detailed in tables Table 2 to Table 4.

In turn, the signals that connect to CN1 are provided in the main from three banks of the User FPGA, Banks 9, 11 and 13. These banks share a common VCCO that can be 2.5V or 3.3V powered, selectable under user control.

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
N_1	F35	1	2	C34	N_2
P_1	G35	3	4	D34	P_2
N_3	F36	5	6	D36	P_4
P_3	G36	7	8	E36	N_4
N_5	E34	9	10	D37	N_6
P_5	F34	11	12	E37	P_6
N_7	J32	13	14	M32	N_8
P_7	K32	15	16	N32	P_8
P_9	M31	17	18	J36	P_10
N_9	N30	19	20	J37	N_10
N_11	K33	21	22	K34	N_12
P_11	L33	23	24	L34	P_12
N_13	V25	25	26	G37	P_14
P_13	W26	27	28	H37	N_14
N_15	M33	29	30	V27	P_16
P_15	N33	31	32	W27	N_16
N_17	U28	33	34	P32	N_18
P_17	V28	35	36	R32	P_18
S_1	D35	37	38	M35/N35	CLK0
+3.3V		39	40	L35/N34	CLK1
+3.3V		41	42		XRM_SERID
+3.3V		43	44		RESERVED
+5V		45	46		XRM_VREF
+5V		47	48		XRM_VCCIO
VBAT		49	50		XRM_VCCIO
+12V		51	52		XRM_VCCIO
+12V		53	54		-12V
PRESENCE_L		55	56		XRM_TDI
XRM_TCK		57	58		XRM_TRST
XRM_TMS		59	60		XRM_TDO

Table 2 XRM Interface - part 1

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
N_19	T31	61	62	U30	N_20
P_19	R31	63	64	U31	P_20
N_21	V29	65	66	P36	N_22
P_21	V30	67	68	R36	P_22
N_23	K36	69	70	P35	N_24
P_23	K37	71	72	R34	P_24
N_25	T36	73	74	W34	P_26
P_25	U36	75	76	W35	N_26
P_27	M37	77	78	Y36	N_28
N_27	N37	79	80	W36	P_28
N_29	V33	81	82	W32	P_30
P_29	V34	83	84	Y33	N_30
N_31	P37	85	86	U35	N_32
P_31	R37	87	88	V35	P_32
CLK2	U33/T30	89	90	U27	S_4
CLK3	U32/T29	91	92	AA25	S_5
S_2	J34	93	94	AA24	S_6
S_3	P31	95	96	AC32	S_7
CLK4	AD29/AE36	97	98	W29	N_34
CLK5	AE29/AD36	99	100	W30	P_34
N_33	Y26	101	102	AE32/AF35	CLK6
P_33	AA26	103	104	AD32/AG35	CLK7
S_8	H33	105	106	AH30	S_10
S_9	H32	107	108	H20	XRM_CLKIN_N
RESERVED		109	110	H19	XRM_CLKIN_P
RESERVED		111	112		XRM_SDA
XRM_PECL_N		113	114		XRM_SCL
XRM_PECL_P		115	116		
RESERVED		117	118		
RESERVED		119	120		

Table 3 XRM Interface - part 2

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
P_35	AA36	121	122	Y32	P_36
N_35	AB36	123	124	Y31	N_36
N_37	AA23	125	126	AB28	P_38
P_37	AB23	127	128	AB27	N_38
P_39	AA35	129	130	AA31	P_40
N_39	AB35	131	132	AA30	N_40
N_41	AB25	133	134	Y27	N_42
P_41	AB26	135	136	AA28	P_42
P_43	AA29	137	138	AE33	N_44
N_43	Y29	139	140	AF33	P_44
P_45	AD35	141	142	AC29	N_46
N_45	AD34	143	144	AC30	P_46
N_47	AD37	145	146	AF31	P_50
P_47	AE37	147	148	AG31	N_50
P_49	AF36	149	150	AJ35	N_48
N_49	AG36	151	152	AH35	P_48
P_51	AD31	153	154	AD27	N_52
N_51	AD30	155	156	AC28	P_52
N_53	AH37	157	158	AF28	N_54
P_53	AG37	159	160	AG28	P_54
P_55	AJ37	161	162	AG32	N_56
N_55	AK37	163	164	AG33	P_56
N_57	AM36	165	166	AN34	N_58
P_57	AL36	167	168	AN35	P_58
N_59	AJ34	169	170	AK32	N_60
P_59	AH34	171	172	AK33	P_60
N_61	AM35	173	174	AN33	N_62
P_61	AL35	175	176	AM33	P_62
N_63	AN37	177	178	AG30	N_64
P_63	AM37	179	180	AF30	P_64

Table 4 XRM Interface - part 3

6.2 XRM Interface – MGT Links

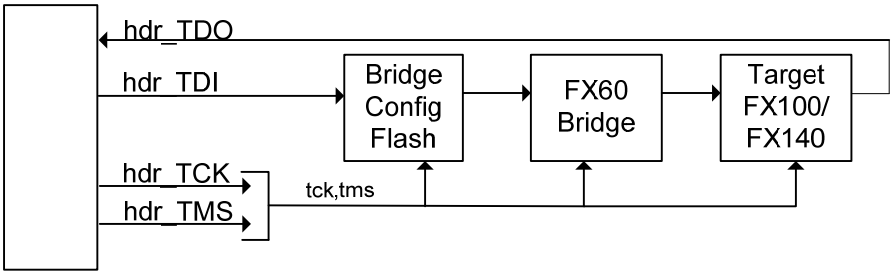
Four lanes of user MGT links are routed to the XRM interface through a Samtec QSE-DP connector U18, as shown in Table 5 below.

Signal	FPGA Pin	MGT Number	Location (FX100)	Location (FX140)	Samtec Pin
XRM_TX1_P	A36	102B	GT11_X0Y6	GT11_X0Y8	1
XRM_TX1_N	A37	"	"	"	3
XRM_RX1_P	C39	"	"	"	2
XRM_RX1_N	D39	"	"	"	4
XRM_TX2_P	M39	103A	GT11_X0Y5	GT11_X0Y7	5
XRM_TX2_N	N39	"	"	"	7
XRM_RX2_P	J39	"	"	"	6
XRM_RX2_N	K39	"	"	"	8
XRM_TX3_P	P39	103B	GT11_X0Y4	GT11_X0Y6	9
XRM_TX3_N	R39	"	"	"	11
XRM_RX3_P	U39	"	"	"	10
XRM_RX3_N	V39	"	"	"	12
XRM_TX4_P	AP39	105A	GT11_X0Y3	GT11_X0Y3	13
XRM_TX4_N	AR39	"	"	"	15
XRM_RX4_P	AL39	"	"	"	14
XRM_RX4_N	AM39	"	"	"	16
XRM_TX5_P	AT39	105B	GT11_X0Y2	GT11_X0Y2	17
XRM_TX5_N	AU39	"	"	"	19
XRM_RX5_P	AW37	"	"	"	18
XRM_RX5_N	AW36	"	"	"	20
XRM_TX6_P	AW28	106A	GT11_X0Y1	GT11_X0Y1	21
XRM_TX6_N	AW27	"	"	"	23
XRM_RX6_P	AW31	"	"	"	22
XRM_RX6_N	AW30	"	"	"	24
XRM_TX7_P	AW25	106B	GT11_X0Y0	GT11_X0Y0	25
XRM_TX7_N	AW24	"	"	"	27
XRM_RX7_P	AW22	"	"	"	26
XRM_RX7_N	AW21	"	"	"	28

Table 5 XRM Interface - MGT Links

7 JTAG Access

The ADPE-XRC-4 provides JTAG access for the fabric of the board through J1. This header will connect to Xilinx download cables using 3V3 signalling levels and has the following devices present in the scan chain :-



The standard ADPE-XRC-4 is configured with the JTAG chain as shown in the table below.

TDI->	XCF32	
	V4FX60	
	V4FX100/140	-> TDO

7.1 JTAG Header (J1)

The table below shows the pin-out for J1, the primary JTAG connector.

Pin	Function
1	+3V3
2	GND
3	FBS **
4	TCK
5	TDO
6	TDI
7	TMS

** The FBS link can be used to disable the boot from flash feature for the target FPGA by linking to the adjacent ground connection on pin 2.