
Summary

The **ADPe-XRC-4** is a high performance reconfigurable PCI Express® card based on the Xilinx™ Virtex-4 FX range of Platform FPGAs. Features include high speed PCI Express® interface, external memory, high density I/O, programmable clocks, temperature monitoring, battery backed encryption (by using an appropriate XRM) and flash boot facilities.

A comprehensive cross platform API with support for **Microsoft Windows™**, **Linux** and **VxWorks** provides access to the full functionality of these hardware features.

Features
Target Devices:

Xilinx Virtex-4 - FX100, FX140 (FF1517)

Memory:

SDRAM - 1GByte in 4 independent banks

FLASH - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.

Front Connector I/O:

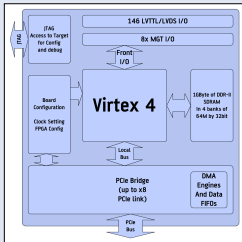
Up to 146 LVTTTL/LVDS I/O

Programmable signaling levels of 1.8V, 2.5V or 3.3V

8 High-Speed Serial Links

8 x 3.125GHz MGTs

Programmable signaling levels of 1.8V, 2.5V or 3.3V



| Compatible Products | | | | | |
|---------------------|-------------------------------------|----------------|------------------------------------|----------------|----------------------------------|
| XRM-ADC-02-125 | Dual 14-bit ADC Interface (125Mbps) | XRM-ADC-03-1GG | Dual 8-bit ADC Interface (1.5Gbps) | XRM-ADC-06-250 | Dual Channel ADC 250Mbps |
| XRM-ADC-04-3G | Single 8-bit ADC I/F (3Gbps) | XRM-CAMERALINK | Single Cameralink Interface | XRM-CLINK-MINI | Single/Dual Cameralink Interface |
| XRM-CLINK-ADV | Cameralink and JPEG2000 | XRM-DAC-03-275 | Dual Channel 14-bit DAC | XRM-DAC-04-1G | Dual Channel 16-bit DAC |
| XRM-DVI-D-RX | DVI Video Capture | XRM-HD-SDI | Dual HDTV I/O Interface | XRM-ID146 | High Density Digital I/O |
| XRM-IC34 | Digital I/O | | | | |

Specification

| | |
|----------------------|--|
| Product Name | ADPe-XRC-4 |
| Target Devices | Xilinx Virtex-4 - FX100, FX140 (FF1517) |
| Host I/F | PCI Express® x8 |
| Interface | PCI Express® x1, x4, x8 link Twin DMA Controllers |
| Memory | SDRAM - 1GByte in 4 independent banks FLASH - Configuration Flash providing an initialisation design for automatic loading into the target FPGA. |
| Front I/O | Up to 146 LVTTTL/LVDS I/O Programmable signaling levels of 1.8V, 2.5V or 3.3V8 High-Speed Serial Links 8 x 3.125GHz MGTs Programmable signaling levels of 1.8V, 2.5V or 3.3V |
| Clocks | Local bus clock programmable up to 100MHz High performance low-jitter LVPECL user clock, programmable up to 500MHz Additional 200MHz reference clock for IOB delay circuits. |
| Device Configuration | PCI Express® Bus direct to SelectMAP port From Flash direct on power up External JTAG connector |
| Software | Drivers for Microsoft Windows™, Linux and VxWorks API with template designs in VHDL and Verilog |
| Environmental | Temperature: Air cooled option (AC0) Operating Temperature 0° to +55°C Air cooled industrial option (AC1) Operating Temperature -20° to +55°C EMC: FCC 47CFR Part 2 EN55022 Equipment Class B |

Ordering Codes
ADPe-XRC-4/z-y(c)

| | | |
|-----------------------|---|--|
| Virtex-4 device | z | FX100, FX140 |
| Virtex-4 speed | y | 10, 11, 12 |
| Air cooled (comm/ind) | c | blank = air cooled commercial, /AC1 = air cooled industrial |

Address: 4 West Silvermills Lane,
Edinburgh, EH3 5BD, UK
Telephone: +44 131 558 2600
Fax: +44 131 558 2700
email: sales@alpha-data.com
website: <http://www.alpha-data.com>

Address: 3507 Ringsby Court Suite 105,
Denver, CO 80216
Telephone: (303) 954 8768
Fax: (866) 820 9956 toll free
email: sales@alpha-data.com
website: <http://www.alpha-data.com>