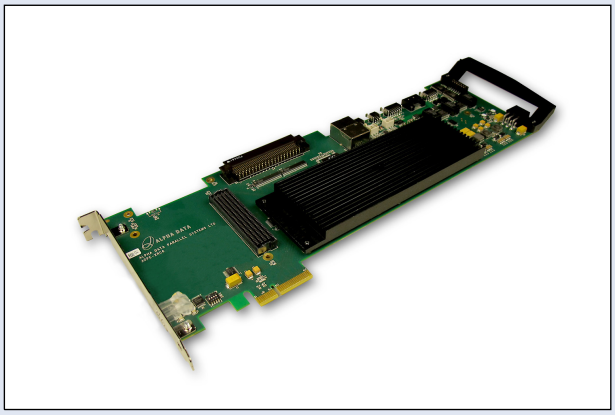
ADPE-XRC-6T

ALPHA DATA

8th May 2012 **Datasheet Revision: 1.0**



Summary

The **ADPE-XRC-6T** is a high performance reconfigurable PCI Express® card based on the Xilinx™ Virtex-6 LXT and SXT ranges of Platform FPGAs. Features include PCI Express® Gen2 interface, external memory, High Pin Count (HPC) VITA 57 FMC I/O, temperature monitoring and flash boot facilities.
A comprehensive cross platform API with support for **Microsoft Windows™**, **Linux** and **VxWorks** provides access to the full functionality of these hardware features.
The **ADPE-XRC-6T-L** has no build options. It has a x1 PCI Express® interface, **256MBytes** of DDR3, has an **LX130T-1** target FPGA and it's cooling option is air cooled commercial only.

Features

Applications:

Radar/Sonar Beamforming
ELINT
Image/Video Processing
Data Encryption

Target Devices:

Xilinx Virtex-6 - LX130T, LX195T, LX240T, LX365T, SX315T, SX475T (FFG1156)

Memory:

SDRAM - 2 independent banks of DDR3 SDRAM @ 800MT/s (32-bit wide 3.2GB/s)
ADPE-XRC-6T-L - 256MBytes
ADPE-XRC-6T - Default memory 1GByte, Option to have 2GByte

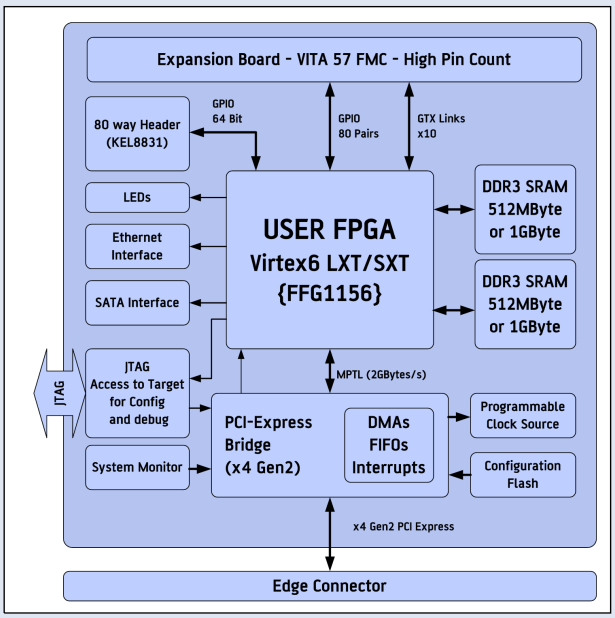
FLASH - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.

Front Connector I/O:

High Pin Count (HPC) FMC Standard Connector:
GPIO 80 pairs
GTX Links x10

Rear Connector I/O:

Secondary Connector (KEL8831):
GPIO 64 signals
Gigabit Ethernet (RJ45)
SATA Interface



ADPE-XRC-6T

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Specification	
Product Name	ADPE-XRC-6T
Target Devices	Xilinx Virtex-6 - LX130T, LX195T, LX240T, LX365T, SX315T, SX475T (FFG1156)
Host I/F	PCI Express Gen2 x4
Interface	PCI Express® Gen2 x4 link to separate bridge device with 5Gb/s local link to user FPGA 4 DMA Controllers Interrupt Controller (Build option to provide a lower capacity Gen2 x1 PCI Express® link and 2 DMA engines -**ADPE-XRC-6T-L**)
Memory	**SDRAM** - 2 independent banks of DDR3 SDRAM @ 800MT/s (32-bit wide 3.2GB/s) ADPE-XRC-6T-L - 256MBytes ADPE-XRC-6T - Default memory 1GByte, Option to have 2GByte **FLASH** - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.
Front I/O	High Pin Count (HPC) FMC Standard Connector: GPIO 80 pairs GTX Links x10
Rear I/O	Secondary Connector (KEL8831): GPIO 64 signals Gigabit Ethernet (RJ45) SATA Interface
Special Functions	Standard VITA 57 FMC IO Module Interface
Clocks	Low-jitter programmable reference clock (default 150MHz for SATA interface) Custom clock inputs available through the FMC interface
Device Configuration	PCI Express® direct to SelectMAP port From Flash direct on power up External JTAG connector
Software	Drivers for Microsoft Windows™, Linux and VxWorks The ADM-XRC Gen3 SDK provides the example C and HDL source code, giving software engineers and FPGA designers a head start in creating applications.
Environmental	**Temperature:** **Air cooled option (AC0)** Operating Temperature 0° to +55°C **Air cooled industrial option (AC1)** Operating Temperature -20° to +55°C **EMC:** FCC 47CFR Part 2 EN55022 Equipment Class B

Ordering Codes		
ADPE-XRC-6T(l)/z-y(m)(c)		
Low Performance	l	blank=Standard PCI Express® interface,-L=Low cost PCI Express Interface
Virtex-6 device	z	LX130T, LX195T, LX240T, LX365T, SX315T, SX475T
Virtex-6 speed	y	1, 2, 3
Memory	m	blank=256MBytes (-L boards) or 1GByte (standard boards), /2=2GBytes
Cooling	c	blank = air cooled commercial, /AC1 = air cooled industrial
Note	#	not all FPGA speed grades available in all configurations. Contact Alpha Data for full details.

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