
Summary

The **XRM-ADC-D10** is an I/O Module which provides two Analog to Digital converters with 16-bit resolution at sampling rates up to 250MHz.

The XRM is aimed at IF/Baseband Signal Sampling. An external clock source may be used or an internally generated clock can be used to provide the sampling clock. An Auxiliary I/O port is provided for use as a trigger input and general purpose signaling. An additional two ports are available for use as high-speed interconnect between boards for synchronisation.

Features
Applications:

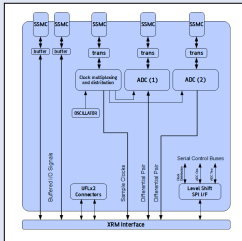
IF/Baseband Signal Sampling

Front Connector I/O:

Dual ADC Input

Clock In

Auxiliary I/O port





Specification

Product Name	XRM-ADC-D10
Front I/O	<p>Signal Input: Dual ADC Input $f_{max} = 250\text{Mpsps}$ resolution = 16-bit bandwidth = 4.5MHz to 700MHz levels = +10dBm impedance = 50 Ohm connector = SSMC</p> <p>Note: exceeding the maximum signal limit may result in permanent degradation of converter performance.</p> <p>Clock In: Clock In $f_{clock} = F_{max}$ levels = 3v3 impedance = Impedance?</p> <p>Note: Exceeding the maximum voltage limit may result in permanent degradation of converter</p> <p>Aux I/O Port: Auxiliary I/O port levels = 2V5 Logic (dc coupled) connector = UFL</p> <p>User configurable as inputs or outputs, signals direct to FPGA pins.</p> <p>Note: signals on these connectors must be restricted to 2V5 logic otherwise damage may result.</p>
XRM2	The XRM-ADC-D10 is also available for XRM2 based FPGA products.
Software	Example UCF, HDL files and Application software are provided with the board.
Environmental	<p>Temperature: Air cooled option Operating Temperature 0° to +55°C†</p> <p>† - It is essential that sufficient air-cooling is provided, if thermal monitoring is provided on board then this should be used to shut the device down if it starts to overheat in order to reduce the possibility of damaging the devices.</p> <p>EMC: FCC 47CFR Part 2 EN55022 Equipment Class B</p>

Ordering Codes

XRM(xver)-ADC-D10

XRM Version	xv- er	blank=Original XRM (FPGA products up to Virtex-5), 2=xRM Version 2 (FPGA products Virtex-6 and later)
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Address: 4 West Silvermills Lane,
 Edinburgh, EH3 5BD, UK
 Telephone: +44 131 558 2600
 Fax: +44 131 558 2700
 email: sales@alpha-data.com
 website: <http://www.alpha-data.com>

Address: 3507 Ringsby Court Suite 105,
 Denver, CO 80216
 Telephone: (303) 954 8768
 Fax: (866) 820 9958 toll free
 email: sales@alpha-data.com
 website: <http://www.alpha-data.com>