XRM-ADC-D3/1G5

Two Channel High Speed Data Acquisition Module

User Guide

Version 1.2

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EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications

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Photo

1. Introduction

The XRM-ADC-D3/1G5 is a front panel adapter card designed principally for use with Alpha Data's ADM-XRC4 and ADM-XRC5 FPGA-based PMC cards, although some limited functionality is possible with the ADM-XP PMC card.

The XRM-ADC-D3/1G5 is based on the ADC08D1500 from National Semiconductor and provides two channels of analogue to digital conversion with 8 bit resolution at sampling rates up to 1.5 GHz It is aimed at applications such as IFSignal Sampling.

An external clock source may be used or an internally generated clock can be used to provide the sampling clock

An auxiliary I/O port is provided for use as a trigger input and general purpose signalling. An additional two ports are available for use as high-speed interconnect between boards for synchronisation.

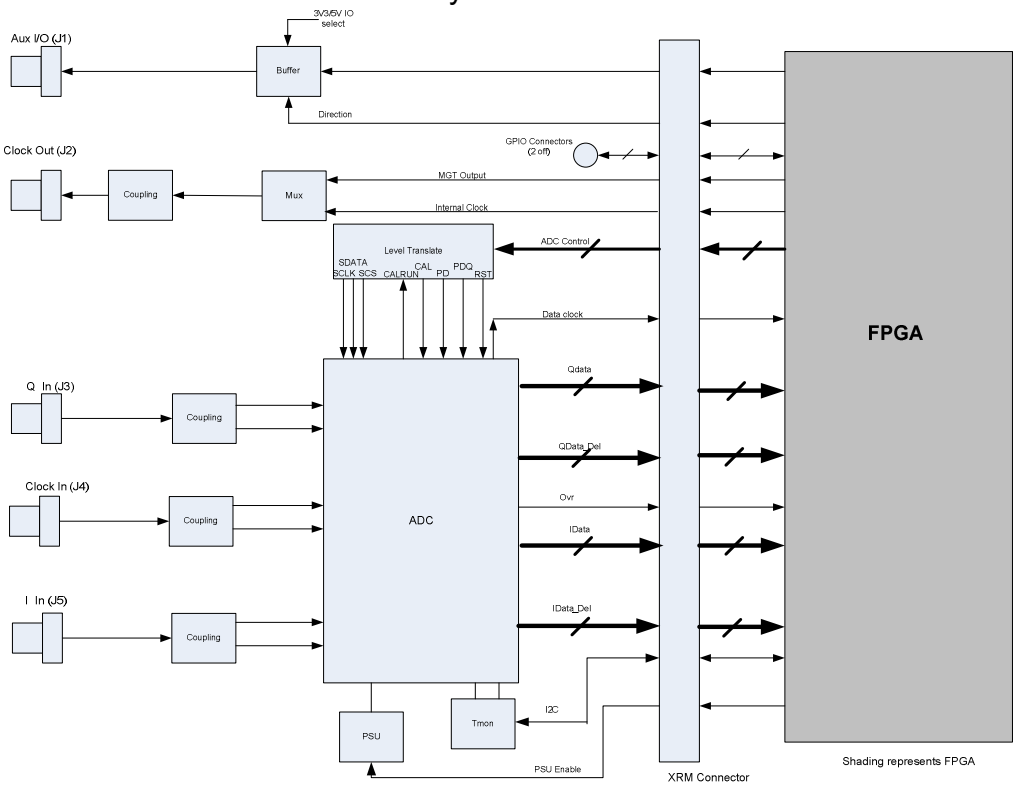


Figure 1 XRM Block Diagram

2. Installation

The XRM-ADC-D3/1G5 is designed to plug in to the front panel connector (SAMTEC QSH series) on the XRC series of cards. The retaining screws should be tightened to secure the XRM-ADC-D3/1G5.

Note: This operation should not be performed while the PMC card is powered up.

2.1. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

3. Specification

3.1. Inputs

3.1.1. I Signal (J5), Q Signal (J3)

Input:	50 Ohms
Bandwidth:	30 MHz to 1700 MHz
Level (Range1):	+/- 435 mV nominal
Level (Range2):	+/- 325 mV nominal

Range selectable via FPGA and ADC serial port.

Note: exceeding the maximum limit may result in permanent degradation of converter performance.

3.1.2. Clock In (J4)

Input: 50 Ohms, ac coupled
Level: +/- 500 mV nominal.
+/- 200 mV minimum to +/1V maximum
Clock Rate:
200 MHz to 1500 MHz , single edge sampling mode
500 MHz to 1500 MHz , dual edge sampling mode

Note: exceeding the maximum voltage limit may result in permanent degradation of converter performance.

3.2. Input /Output

3.2.1. Clock Out (J2)

Impedance: 50 Ohms, ac coupled
Level: +/- 400 mV nominal.
Source: GTP or User Clock from XRC board.
Clock Rate:
20 MHz to 500 MHz , User Clock
300 MHz to 1500 MHz GTP

3.2.2. Aux IO Port (J1)

User configurable as input or output
Input: 4k7 Ohms, dc coupled
Level: +3V3 LVTTL or +5V TTL (factory/user selectable[1])

[1] configured via 0R links

3.2.3. Synch Ports (J6 and J7)

User configurable as input or output, direct to FPGA pins.
Input: dc coupled
Level: 2V5 logic

Note: signals on these connectors must be restricted to 2V5 logic levels else damage may result.

4. Options

4.1. Connector type

SMA (7 mm, standard)
Long Barrel SMA (20 mm)
SMB
SMC

4.2. Order Code

XRM-ADC-D3/1G5 –[Connector option] -[IO voltage option]

Fields in square brackets may be omitted in order to obtain the standard configuration for that option. For custom filter designs or other customisation requirements (e.g. connectors) please contact Alpha Data.

5. Related Documents

ADM-XRC4SX User Manual
ADM-XRC4LX User Manual
ADM-XMC4FX User Manuals
ADM-XRC5LX User Manual
ADM-XRC5T1 User Manual
ADM-XRC5T2 User Manual
ADM-XRC5TZ User Manual
ADM-XRC6TL User Manual
ADM-XRC6T1 User Manual
ADM-XRC6TGE User Manual

ADC-HS Example Code Description

6. Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

7. Pinout

Pin No.	UCF Name	XRC 4LX	XRC 4SX	XRC 4FX	ADPE 4FX	Comments
18	adc_psuen	k28	k28	j26	j37	
2	tmon_alert_l	d32	d32	l28	c34	
4	tmon_temp_data	c32	c32	k28	d34	
6	tmon_temp_ck	n22	n22	j29	e36	
8	adc_cntrl_oe_l	n23	n23	h29	d36	
10	adc_cntrl_pwdnq	j30	j30	f29	d37	
9	adc_cntrl_cal	h30	h30	f28	e34	
11	adc_cntrl_pwdn	h29	h29	e28	an7	
12	adc_cntrl_cal_active	j29	j29	e29	e3	
1	adc_cntrl_scs_l	h28	h28	c27	f35	
3	adc_cntrl_sck	h27	h27	c28	g35	
5	adc_cntrl_sdata	k27	k27	l29	f36	
26	mux_sel<0>	m32	m32	d26	h37	
28	mux_sel<1>	m33	m33	e26	g37	
29	auxio_dirn	r19	r19	d31	m33	
35	auxio	p24	p24	g33	v28	
38	gpio_p	f33	d34	f25	m35	
40	gpio_n	f34	e34	f24	l35	
102	adc_ckz_p	aa25	am21	v37	ae32	
104	adc_ckz_n	aa26	am22	u37	ad32	
87	adc_ovr_p	p30	ac29	n30	r37	
85	adc_ovr_n	p31	ac30	m31	p37	
83	qdata_p<0>	p29	ae33	l34	v34	
81	qdata_n<0>	r29	ae34	k34	v33	
100	qdata_p<1>	u30	af31	h37	w30	
98	qdata_n<1>	u31	ae31	g37	w29	
103	qdata_p<2>	u32	aj34	n33	aa26	
101	qdata_n<2>	u33	ah34	m33	y26	
122	qdata_p<3>	w32	ah32	r31	y32	
124	qdata_n<3>	v32	ah33	t31	y31	
121	qdata_p<4>	v23	ag30	r32	aa36	
123	qdata_n<4>	v24	ag31	p32	ab36	
127	qdata_p<5>	w27	ak33	m35	ab23	
125	qdata_n<5>	v27	ak34	l35	aa23	
135	qdata_p<6>	ab31	am31	w26	ab26	
133	qdata_n<6>	aa31	al31	v25	ab25	
140	qdata_p<7>	aj34	ap27	n37	af33	
138	qdata_n<7>	ah34	an27	m37	ae33	
146	qdatadel_p<0>	ab30	af26	w36	af31	
148	qdatadel_n<0>	aa30	ae26	y36	ag31	
136	qdatadel_p<1>	y27	aj30	v30	aa28	
134	qdatadel_n<1>	y28	ah30	v29	y27	
126	qdatadel_p<2>	y29	am32	u33	ab28	
128	qdatadel_n<2>	w29	am33	u32	ab27	
130	qdatadel_p<3>	aa33	al33	v28	aa31	
132	qdatadel_n<3>	aa34	al34	u28	aa30	
144	qdatadel_p<4>	aa28	ak29	r36	ac30	
142	qdatadel_n<4>	aa29	aj29	p36	ac29	
147	qdatadel_p<5>	ae33	ak21	r37	ae37	
145	qdatadel_n<5>	ae34	al21	p37	ad37	
141	qdatadel_p<6>	aa23	ap21	k37	ad35	
143	qdatadel_n<6>	aa24	ap22	k36	ad34	
129	qdatadel_p<7>	ab32	ab22	u31	aa35	

131	qdatadel_n<7>	ab33	ab23	u30	ab35	
176	idata_p<0>	ak33	al26	ab26	am33	
174	idata_n<0>	ak34	ak26	ab25	an33	
179	idata_p<1>	aj30	an25	aa29	am37	
177	idata_n<1>	ah30	am25	y29	an37	
175	idata_p<2>	am32	ag23	ab28	al35	
173	idata_n<2>	am33	af24	ab27	am35	
171	idata_p<3>	ah32	ag25	aa26	ah34	
169	idata_n<3>	ah33	ag26	y26	aj34	
167	idata_p<4>	al33	am26	y32	al36	
165	idata_n<4>	al34	am27	y31	am36	
161	idata_p<5>	ac32	ah28	aa35	aj37	
163	idata_n<5>	ac33	ah29	ab35	ak37	
153	idata_p<6>	ad27	ap29	w32	ad31	
155	idata_n<6>	ac27	an29	y33	ad30	
149	idata_p<7>	ag32	ak22	v34	af36	
151	idata_n<7>	ag33	ak23	v33	ag36	
164	idatadel_p<0>	af31	aj27	w30	ag33	
162	idatadel_n<0>	ae31	ah27	w29	ag32	
168	idatadel_p<1>	af33	al28	ab23	an35	
166	idatadel_n<1>	af34	al29	aa23	an34	
152	idatadel_p<2>	ac29	ap30	r34	ah35	
150	idatadel_n<2>	ac30	an30	p35	aj35	
156	idatadel_p<3>	w24	af28	w35	ac28	
154	idatadel_n<3>	y24	ae27	w34	ad27	
160	idatadel_p<4>	ae32	am30	aa36	ag28	
158	idatadel_n<4>	ad32	al30	ab36	af28	
159	idatadel_p<5>	ae29	ap25	y34	ag37	
157	idatadel_n<5>	ad29	ap26	aa34	ah37	
172	idatadel_p<6>	ab22	ap24	aa31	ak33	
170	idatadel_n<6>	ab23	an24	aa30	ak32	
180	idatadel_p<7>	am31	al23	aa28	af30	
178	idatadel_n<7>	al31	am23	y27	ag30	

Pin No.	**UCF Name**	**XRC 5LX**	**XRC 5T1**	**XRC 5T2**	**Comments**
18	adc_psuen	AN10	AK11	N39	
2	tmon_alert_l	AN4	AA10	J38	
4	tmon_temp_data	AN5	AB10	K38	
6	tmon_temp_ck	AP5	AA8	K40	
8	adc_cntrl_oe_l	AP4	AA9	K39	
10	adc_cntrl_pwdnq	AM7	AM11	U38	
9	adc_cntrl_cal	AM6	AB8	P37	
11	adc_cntrl_pwdn	AN7	AC8	R37	
12	adc_cntrl_cal_active	AM8	AM12	T37	
1	adc_cntrl_scs_l	AL6	AP14	Y34	
3	adc_cntrl_sck	AL5	AN14	AA34	
5	adc_cntrl_sdata	AL4	AM13	W35	
26	mux_sel<0>	AM15	AH9	M38	
28	mux_sel<1>	AM16	AH10	L39	
29	auxio_dirn	AN14	AH8	H39	
35	auxio	AA10	AC4	F41	
38	gpio_p	AP9	AD10	H40	
40	gpio_n	AP10	AD11	J40	
102	adc_ckz_p	AG1	T8	AV40	
104	adc_ckz_n	AG2	U7	AU39	

87	adc_ovr_p	AJ10	AK7	AA42	
85	adc_ovr_n	AH10	AK6	AA41	
83	qdata_p<0>	AK9	AJ7	W42	
81	qdata_n<0>	AK8	AJ6	Y42	
100	qdata_p<1>	W9	F9	AB41	
98	qdata_n<1>	Y9	F8	AB42	
103	qdata_p<2>	Y11	E9	AC40	
101	qdata_n<2>	W11	E8	AC39	
122	qdata_p<3>	V9	G8	AC41	
124	qdata_n<3>	V8	H8	AD42	
121	qdata_p<4>	W10	F10	AJ42	
123	qdata_n<4>	V10	G10	AJ41	
127	qdata_p<5>	W5	K11	AR42	
125	qdata_n<5>	V5	J11	AT42	
135	qdata_p<6>	Y4	J10	AT41	
133	qdata_n<6>	W4	J9	AU41	
140	qdata_p<7>	AF5	F11	AF41	
138	qdata_n<7>	AE6	E11	AF42	
146	qdatadel_p<0>	W1	N8	AE39	
148	qdatadel_n<0>	V2	N7	AE38	
136	qdatadel_p<1>	AB6	B13	AG42	
134	qdatadel_n<1>	AC5	C13	AH41	
126	qdatadel_p<2>	Y7	D12	AB39	
128	qdatadel_n<2>	Y8	C12	AC38	
130	qdatadel_p<3>	AA6	A13	AE42	
132	qdatadel_n<3>	AA5	B12	AD41	
144	qdatadel_p<4>	AF6	E12	AB37	
142	qdatadel_n<4>	AG6	E13	AB38	
147	qdatadel_p<5>	AK4	N10	AP42	
145	qdatadel_n<5>	AJ5	N9	AP41	
141	qdatadel_p<6>	AH4	M10	AU42	
143	qdatadel_n<6>	AJ4	L9	AV41	
129	qdatadel_p<7>	Y6	H10	AL41	
131	qdatadel_n<7>	W6	H9	AK42	
176	idata_p<0>	AN2	G6	AN40	
174	idata_n<0>	AP2	G7	AP40	
179	idata_p<1>	AM2	T9	AB34	
177	idata_n<1>	AL3	U10	AC34	
175	idata_p<2>	AL1	T10	AC36	
173	idata_n<2>	AM1	T11	AD35	
171	idata_p<3>	AK2	H5	AC35	
169	idata_n<3>	AK3	G5	AB36	
167	idata_p<4>	AF1	R7	AD36	
165	idata_n<4>	AE1	R8	AD37	
161	idata_p<5>	AC2	R6	AM37	
163	idata_n<5>	AD1	T6	AL37	
153	idata_p<6>	Y3	M7	AT39	
155	idata_n<6>	Y2	L6	AR39	
149	idata_p<7>	V4	M6	AN39	
151	idata_n<7>	V3	M5	AP38	
164	idatadel_p<0>	AE2	J6	AJ37	
162	idatadel_n<0>	AD2	J5	AH38	
168	idatadel_p<1>	AF3	H7	AL39	
166	idatadel_n<1>	AE3	J7	AM39	
152	idatadel_p<2>	AG5	F13	AH40	
150	idatadel_n<2>	AH5	G13	AJ40	
156	idatadel_p<3>	W2	N5	AF39	
154	idatadel_n<3>	Y1	P5	AG38	
160	idatadel_p<4>	AB3	K7	AN38	
158	idatadel_n<4>	AA3	K6	AM38	
159	idatadel_p<5>	AB1	P7	AG37	
157	idatadel_n<5>	AA1	P6	AF37	
172	idatadel_p<6>	AG3	F5	AJ38	
170	idatadel_n<6>	AH3	F6	AK39	
180	idatadel_p<7>	AM3	E6	AR40	
178	idatadel_n<7>	AN3	E7	AT40	

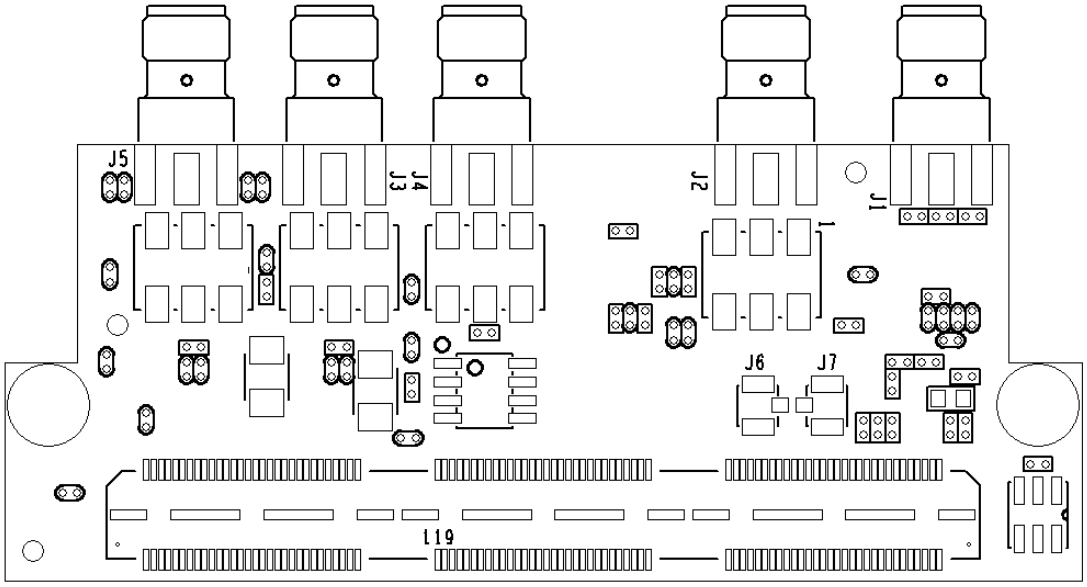
Pin No.	UCF Name	XRC-6TL	XRC-6T1	XRC-6TGE	Comments
18	adc_psuen	M41	M41	M41	
2	tmon_alert_l	M39	M39	M39	
4	tmon_temp_data	M38	M38	M38	
6	tmon_temp_ck	P40	P40	P40	
8	adc_cntrl_oe_l	P41	P41	P41	
10	adc_cntrl_pwdnq	L42	L42	L42	No connection 3G parts
9	adc_cntrl_cal	L40	L40	L40	
11	adc_cntrl_pwdn	L39	L39	L39	
12	adc_cntrl_cal_active	L41	L41	L41	
1	adc_cntrl_scs_l	N39	N39	N39	
3	adc_cntrl_sck	N38	N38	N38	
5	adc_cntrl_sdata	T36	T36	T36	
26	mux_sel<0>	N40	N40	N40	
28	mux_sel<1>	N41	N41	N41	
29	auxio_dirn	M37	M37	M37	
35	auxio	W37	W37	W37	
38	gpio_p	P36	P36	P36	
40	gpio_n	P35	P35	P35	
102	adc_ckz_p	AH34	AH34	AH34	
104	adc_ckz_n	AJ35	AJ35	AJ35	
87	adc_ovr_p	AA35	AA35	AA35	
85	adc_ovr_n	Y35	Y35	Y35	
					ADC Data sheet reference:
83	qdata_p<0>	Y40	Y40	Y40	Cdata_p<0>
81	qdata_n<0>	Y39	Y39	Y39	Cdata_n<0>
100	qdata_p<1>	AB37	AB37	AB37	Cdata_p<1>
98	qdata_n<1>	AB38	AB38	AB38	Cdata_n<1>
103	qdata_p<2>	AC36	AC36	AC36	Cdata_p<2>
101	qdata_n<2>	AB36	AB36	AB36	Cdata_n<2>
122	qdata_p<3>	AA42	AA42	AA42	Cdata_p<3>
124	qdata_n<3>	AB42	AB42	AB42	Cdata_n<3>
121	qdata_p<4>	AC41	AC41	AC41	Cdata_p<4>
123	qdata_n<4>	AD41	AD41	AD41	Cdata_n<4>
127	qdata_p<5>	AC34	AC34	AC34	Cdata_p<5>
125	qdata_n<5>	AC33	AC33	AC33	Cdata_n<5>
135	qdata_p<6>	AE33	AE33	AE33	Cdata_p<6>
133	qdata_n<6>	AD33	AD33	AD33	Cdata_n<6>
140	qdata_p<7>	AE38	AE38	AE38	Cdata_p<7>
138	qdata_n<7>	AD38	AD38	AD38	Cdata_n<7>
146	qdatadel_p<0>	AL42	AL42	AL42	Adata_p<0>
148	qdatadel_n<0>	AM42	AM42	AM42	Adata_n<0>
136	qdatadel_p<1>	AA41	AA41	AA41	Adata_p<1>
134	qdatadel_n<1>	AB41	AB41	AB41	Adata_n<1>
126	qdatadel_p<2>	AB39	AB39	AB39	Adata_p<2>
128	qdatadel_n<2>	AA40	AA40	AA40	Adata_n<2>
130	qdatadel_p<3>	AC40	AC40	AC40	Adata_p<3>
132	qdatadel_n<3>	AD40	AD40	AD40	Adata_n<3>
144	qdatadel_p<4>	AE37	AE37	AE37	Adata_p<4>
142	qdatadel_n<4>	AD37	AD37	AD37	Adata_n<4>
147	qdatadel_p<5>	AE40	AE40	AE40	Adata_p<5>
145	qdatadel_n<5>	AE39	AE39	AE39	Adata_n<5>
141	qdatadel_p<6>	AB32	AB32	AB32	Adata_p<6>
143	qdatadel_n<6>	AB33	AB33	AB33	Adata_n<6>
129	qdatadel_p<7>	AD42	AD42	AD42	Adata_p<7>

131	qdatadel_n<7>	AE42	AE42	AE42	Adata_n<7>
176	idata_p<0>	AF39	AF39	AF39	Ddata_p<0>
174	idata_n<0>	AG39	AG39	AG39	Ddata_n<0>
179	idata_p<1>	AF32	AF32	AF32	Ddata_p<1>
177	idata_n<1>	AG33	AG33	AG33	Ddata_n<1>
175	idata_p<2>	AG34	AG34	AG34	Ddata_p<2>
173	idata_n<2>	AF34	AF34	AF34	Ddata_n<2>
171	idata_p<3>	AH39	AH39	AH39	Ddata_p<3>
169	idata_n<3>	AJ40	AJ40	AJ40	Ddata_n<3>
167	idata_p<4>	AF35	AF35	AF35	Ddata_p<4>
165	idata_n<4>	AF36	AF36	AF36	Ddata_n<4>
161	idata_p<5>	AK40	AK40	AK40	Ddata_p<5>
163	idata_n<5>	AL40	AL40	AL40	Ddata_n<5>
153	idata_p<6>	AJ42	AJ42	AJ42	Ddata_p<6>
155	idata_n<6>	AK42	AK42	AK42	Ddata_n<6>
149	idata_p<7>	AK38	AK38	AK38	Ddata_p<7>
151	idata_n<7>	AJ38	AJ38	AJ38	Ddata_n<7>
164	idatadel_p<0>	AK39	AK39	AK39	Bdata_p<0>
162	idatadel_n<0>	AL39	AL39	AL39	Bdata_n<0>
168	idatadel_p<1>	AG42	AG42	AG42	Bdata_p<1>
166	idatadel_n<1>	AH41	AH41	AH41	Bdata_n<1>
152	idatadel_p<2>	AE34	AE34	AE34	Bdata_p<2>
150	idatadel_n<2>	AE35	AE35	AE35	Bdata_n<2>
156	idatadel_p<3>	AL41	AL41	AL41	Bdata_p<3>
154	idatadel_n<3>	AM41	AM41	AM41	Bdata_n<3>
160	idatadel_p<4>	AF40	AF40	AF40	Bdata_p<4>
158	idatadel_n<4>	AG41	AG41	AG41	Bdata_n<4>
159	idatadel_p<5>	AF37	AF37	AF37	Bdata_p<5>
157	idatadel_n<5>	AG37	AG37	AG37	Bdata_n<5>
172	idatadel_p<6>	AH40	AH40	AH40	Bdata_p<6>
170	idatadel_n<6>	AJ41	AJ41	AJ41	Bdata_n<6>
180	idatadel_p<7>	AJ37	AJ37	AJ37	Bdata_p<7>
178	idatadel_n<7>	AK37	AK37	AK37	Bdata_n<7>

Notes:

1. Analogue data is encoded in offset binary format with 0xFF representing positive full scale and 0x00 representing negative full scale.
2. OVERRANGE goes high when the signal input is outwith the valid ADC input range on either channel.
3. Auxio is routed via a bidirectional buffer which converts FPGA logic levels to either 3V3 or 5V levels. This port defaults to an input when the FPGA is unconfigured.
4. Gpio_n and Gpio_p are connected directly to FPGA IO pins to allow fast signalling between boards. Care should be taken when using these to ensure that the correct logic levels and directions are configured otherwise permanent damage to the FPGA may result.
5. The example UCF files supersede any pinouts above.
6. Other unlisted boards may be supported - see the UCF files in the example code
7. Temperature monitoring of the DAC is provided.
8. Further information on pin functions is contained in the example code.

8. Board Layout



J7 – Synch port
J6 – Synch port
J3 – ADC Clock in
J5 – ADC Signal in, I
J4 – ADC Signal in, Q
J2 – Clock out
J1 – Aux IO

Revision History

Date	Revision	Nature of Change
Dec 2007	1.0	First issue
Feb 09	1.1	Updated block diagram, board layout. Updated pin connections list.
Dec 2012	1.2	Added V6 board pinouts, removed unused pins from list.