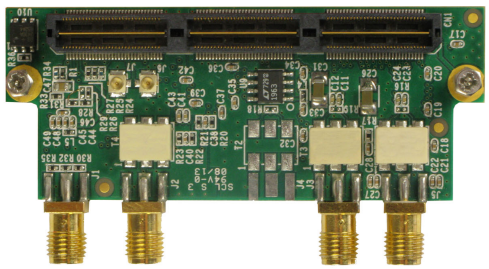
XRM-ADC-S4/3G

ALPHA DATA

9th February 2015 **Datasheet Revision: 1.2**



Summary

The **XRM-ADC-S4/3G** is an I/O Module which provides a single channel Analog to Digital convertor with 8-bit resolution at sampling rates up to 3GHz.

The XRM is aimed at IF/Baseband Signal Sampling. An external clock source may be used or an internally generated clock can be used to provide the sampling clock. An Auxiliary I/O port is provided for use as a trigger input and general purpose signaling. An additional two ports are available for use as high-speed interconnect between boards for synchronisation.
The built-in thermal monitor allows the user to check the operating temperature of the ADC. Provided as part of the sample design is the functionality to read the temperature of the device, and software to monitor this and recalibrate the ADC if the thermal drift is sufficient. The software will also shut the ADC down if the device starts to go over the maximum operating temperature.

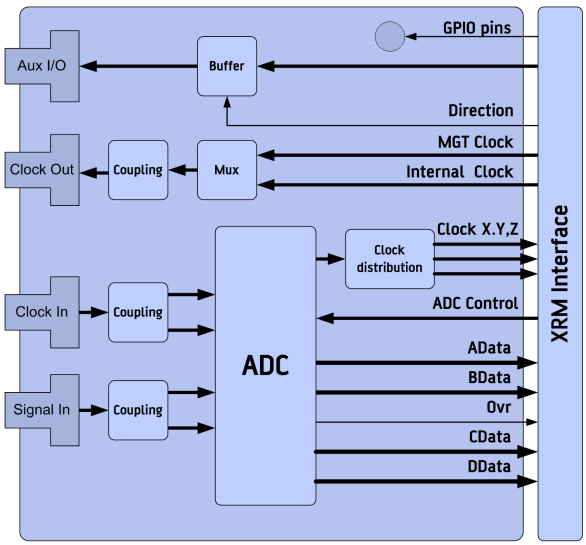
Features

Applications:

- IF/Baseband Signal Sampling

Front Connector I/O:

- Single ADC Input
- Clock In
- Clock Out
- Auxiliary I/O port
- Dual external synchronisation ports



Specification	
Product Name	XRM-ADC-S4/3G
Front I/O	**Signal Input:** Single ADC Input fmax = 3Gsps resolution = 8-Bit bandwidth = 30MHz to 1700MHz nominal levels = Range1: ±410 mV nominal Range2: ±300 mV nominal impedance = 50 Ohm connector = SMA SMA-L SMB SMC Range selectable via FPGA and ADC serial port: bandwidth limited by input transmission-line transformers. ADC 3dB bandwidth 3GHz. **Note:** exceeding the maximum signal limit may result in permanent degradation of converter performance. **Clock In:** Clock In fclock = 200MHz to 1500MHz, single edge sampling 500MHz to 1500MHz, dual edge sampling levels = 424 mV peak to peak (-3.5dBm) nominal, 283 mV peak to peak (-7dBm) minimum up to 1.414 V peak to peak (+7dBm) maximum at SMA connector impedance = 50 Ohms (ac coupled) **Note:** Exceeding the maximum voltage limit may result in permanent degradation of converter **Clock Out:** Clock Out impedance = 50 Ohms, ac coupled levels = ±400mV nominal Source: GTP or User Clock from XRC board. Clock Rate: 20MHz to 500MHz - User clock 300MHz to 1500MHz GTP **Auxiliary I/O:** Auxiliary I/O port impedance = input 4k7 Ohms, dc coupled levels = 3V3 LVTTL or +5V TTL (factory/user selectable) **Sync Ports:** Dual external synchronisation ports levels = 2V5 Logic (dc coupled) User configurable as inputs or outputs, signals direct to FPGA pins. **Note:** signals on these connectors must be restricted to 2V5 logic otherwise damage may result.
XRM2	The XRM-ADC-S4/3G is also available for XRM2 based FPGA products.
Special Functions	The XRM has built-in thermal monitoring of the ADC
Software	Example UCF, HDL files and Application software are provided with the board.
Environmental	**Temperature:** Air cooled option Operating Temperature 0° to +55°C† † - It is essential that sufficient air-cooling is provided, if thermal monitoring is provided on board then this should be used to shut the device down if it starts to overheat in order to reduce the possibilty of damaging the devices. **EMC:** FCC 47CFR Part 2 EN55022 Equipment Class B

Ordering Codes		
XRM(xver)-ADC-S4/3G(con)(h)		
XRM Version	xv-er	blank=Original XRM (FPGA products up to Virtex-5), 2=XRM Version 2 (FPGA products Virtex-6 and later)
Connector Option	con	/blank=SMA (7mm standard), /SMA20= Long Barrel SMA(20mm), /SMB, /SMC
Heatsink	h	blank = No Heastink, /HTSK-XRM-ADC-HS-1 = Heatsink Fitted

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