XRM-DAC-D3/275

Two Channel Data Generation Module

User Guide

Version 1.6

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EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications

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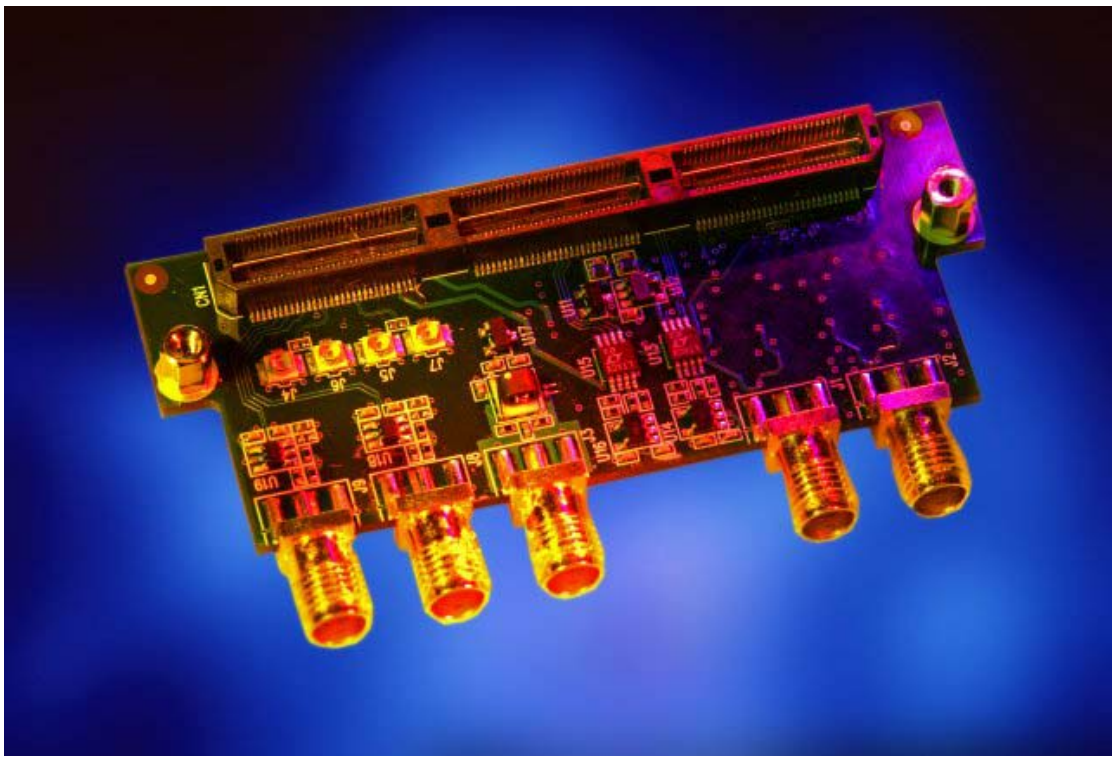


1. Introduction

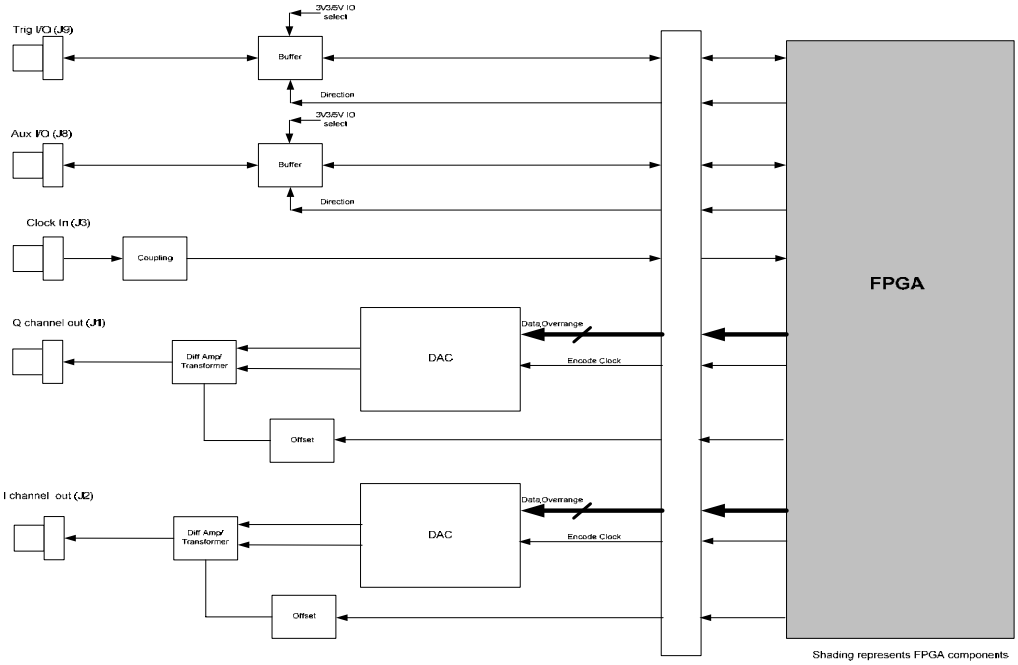
The XRM-DAC-D3/275 is a front panel adapter card designed for use with Alpha Data's ADM-XRCII, ADM-XP, ADM-XRC4 and ADM-XRC5 FPGA-based PMC cards.

The XRM-DAC-D3/275 provides two channels of digital-to-analogue conversion with 14 bit resolution and supports sampling rates in excess of 125 MHz It is aimed at applications such as IF/Baseband Signal generation.

A number of customisation options are offered with this card, including ac-coupling of the analogue outputs for best signal fidelity or dc-coupling for larger voltage swing and offset adjustment.

An external clock source may be used or an internally generated clock can be used to provide the sampling clock

Two auxiliary I/O ports are provided for use as trigger inputs and general purpose signalling.



2. Installation

The XRM-DAC-D3/275 is designed to plug in to the front panel connector (SAMTEC QSH series) on the range of Alpha Data PMC cards indicated above. The retaining screws should be tightened to secure the XRM-DAC-D3/275.

Note: This operation should not be performed while the PMC card is powered up.

2.1. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

2.2. Signalling Voltage

This board uses **3v3** signalling only. The signalling voltage jumper on the host FPGA card should be set accordingly before powering up.

3. Specification

3.1. Outputs

3.1.1. I Signal (J2), Q Signal (J1)

DC Coupled

Output: 50 Ohms
Bandwidth: DC to 80 MHz (3dB)
Level: +/- 0.5V (+4 dBm) = DAC full scale into 50R load.
SFDR : >55dB[1]

AC Coupled

Output: 50 Ohms
Bandwidth: 0.25MHz to 80 MHz (3dB)
Level: +/-0.4V (+2 dBm) = DAC full scale into 50R load.
SFDR : >60dB[1]

3.1.2. Offset

-1 V to +1 V dc, 16 bits resolution each channel,
dc-coupled configuration only.

3.1.3. Sample Rate

1 MHz to 275 MHz[2]

3.2. Clock In (J3)

Input: 50 Ohms, ac coupled
Level: +12 dBm nominal (2.5V pk to pk)

3.3. Input /Output:

3.3.1. Trig IO Port (J9)

User configurable as input or output
Input: 4k7 Ohms, dc coupled
Level: +3V3 LVTTL or +5V TTL (factory/user selectable[3])

[1] XRC4LX running sine wave example code, external clock =100 MHz, Full scale -1dB, Fout=12.5 MHz, 1st Nyquist zone
[2] Maximum sampling frequency is FPGA type and speed dependent. Max sample rate achievable on XRC2 and XP boards is 175 MHz.
[3] Configured via 0R links

3.3.2. Aux. IO Port (J8)

User configurable as input or output
Input: 4k7 Ohms, dc coupled
Level: +3V3 LVTTL or +5V TTL (factory/user selectable[4])

[4] configured via 0R links

4. Options

4.1. Connector type

SMA (7 mm, standard)
Long Barrel SMA (20 mm)
SMB
SMC

4.2. Order Code

XRM-DAC-D3/275–[Coupling]-[Connector option] -[IO voltage option]

Fields in square brackets may be omitted in order to obtain the standard configuration for that option.

5. Related Documents

ADM-XRC-II User Manual
ADM-XP User Manual
ADM-XRC4SX/LX User Manuals
ADM-XRC5 User Manual
ADM-XRC5T1 User Manual
ADM-XRC5T2 User Manual

6. Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

7. Pinout

7.1. Virtex2/Pro

Samtec Pin No.	UCF Name	XRC2	XPL	XP	XPI	Comments
1	SYNTHSEL(3)	C2	F8	D10	D10	
3	SYNTHSEL(2)	B3	F7	E10	E10	
6	TRIG_IO	C9	D8	H13	H13	
9	SYNTHSEL(1)	D6	F10	J10	J10	
10	TRIG_DIRN	B9	A8	M19	M19	
11	SYNTHSEL(0)	C6	F9	H10	H10	
13	SYNTH_OE	H11	G11	G10	G10	
14	AUX_IO	D10	D10	L18	L18	
20	AUX_DIRN	G10	B9	F13	F13	
24	SYNTHREFCK	H9	E11	F9	F9	
26	DEBUG(0)	H12	C10	K13	K13	
28	DEBUG(1)	H13	C11	J13	J13	
38	DEBUG(2)	H16	C15	F21	F21	
40	DEBUG(3)	H17	B15	G21	G21	
89	EXTCK_P	E16	G15	K21	K21	was DEBUG(6), rev2 boards
90	IOFFS_SDI	C16	H19	C19	C19	
91	EXTCK_N	E17	F15	J21	J21	was SYNTHCK, rev2 boards
92	IOFFS_CK	D17	C23	D19	D19	
94	IOFFS_LD	D18	D23	E28	E28	
97	DEBUG(6)	J18	G22	G22	G22	was EXTCK_P, rev2 boards
99	SYNTHCK	K18	H22	H22	H22	was EXTCK_N, rev2 boards
102	DEBUG(4)	E18	C24	J22	J22	
103	QOFFS_SDI	F19	E24	G27	G27	
104	DEBUG(5)	E19	D24	K22	K22	
105	QOFFS_CK	G20	F23	J27	J27	
107	QOFFS_LD	A28	E23	K27	K27	
122	DAC_Q(13)	K22	AF4	C30	C30	
124	DAC_Q(12)	K23	AF3	D30	D30	
126	DAC_Q(11)	H20	AF2	M26	M26	
128	DAC_Q(10)	H21	AF1	M25	M25	
130	DAC_Q(9)	J21	AD4	J26	J26	
132	DAC_Q(8)	J22	AD3	H26	H26	
134	DAC_Q(7)	D20	AB6	J24	J24	
136	DAC_Q(6)	D21	AB5	K24	K24	
138	DAC_Q(5)	E21	AC6	C23	C23	
140	DAC_Q(4)	E22	AC5	D23	D23	
142	DAC_Q(3)	B21	J26	G24	G24	
144	DAC_Q(2)	B22	J25	H24	H24	
146	DAC_Q(1)	H22	Y23	K30	K30	
148	DAC_Q(0)	H23	Y24	J30	J30	
149	DACI_CLK	J23	F28	C32	C32	
150	DACQ_CLK	D22	H26	K25	K25	
154	DAC_I(13)	C22	AB25	E24	E24	
156	DAC_I(12)	C23	AB26	F24	F24	
158	DAC_I(11)	B23	E28	K23	K23	
160	DAC_I(10)	B24	E27	L23	L23	
162	DAC_I(9)	F23	AC25	G30	G30	
164	DAC_I(8)	F24	AC26	H30	H30	
166	DAC_I(7)	C24	E30	G25	G25	
168	DAC_I(6)	D24	E29	H25	H25	
170	DAC_I(5)	G24	AE29	G31	G31	
172	DAC_I(4)	G25	AE30	F31	F31	
174	DAC_I(3)	D25	AF29	L30	L30	
176	DAC_I(2)	D26	AF30	M30	M30	
178	DAC_I(1)	K21	H28	J23	J23	
180	DAC_I(0)	K20	H27	H23	H23	

7.2. Virtex 4

Samtec Pin No.	UCF Name	V4SX	V4LX	V4FX	ADPE4FX	Comments
1	SYNTHSEL(3)	H28	H28	AL6	F35	
3	SYNTHSEL(2)	H27	H27	AL5	G35	
6	TRIG_IO	N22	N22	AP5	E36	
9	SYNTHSEL(1)	H30	H30	AM6	E34	
10	TRIG_DIRN	J30	J30	AM7	D37	
11	SYNTHSEL(0)	H29	H29	AN7	F34	
13	SYNTH_OE	E33	E33	AN8	J32	
14	AUX_IO	R21	R21	AL10	M32	
20	AUX_DIRN	K29	K29	AM11	J36	
24	SYNTHREFCK	L30	L30	AP16	L34	
26	DEBUG(0)	M32	M32	AM15	H37	
28	DEBUG(1)	M33	M33	AM16	G37	
38	DEBUG(2)	F33/D34	F33/D34	AP9	N35	
40	DEBUG(3)	F34/E34	F34/E34	AP10	N34	
89	EXTCK_P	AC32/AD34	R32/P34	AE8	T30	was DEBUG(6), rev2 boards
90	IOFFS_SDI	AA24	V34	AH9	U27	
91	EXTCK_N	AC33/AC34	R33/R34	AF8	U32	was SYNTHCK, rev2 boards
92	IOFFS_CK	AA23	V33	W7	AA25	
94	IOFFS_LD	AD29	U27	AE4	AA24	
97	DEBUG(6)	AK24/AL24	AG30/AF29	AA4	AE36	was EXTCK_P, rev2 boards
99	SYNTHCK	AJ24/AL25	AG31/AF30	T36	AD36	was EXTCK_N, rev2 boards
102	DEBUG(4)	AN22/AM21	AC28/AA25	AG1	AE32	
103	QOFFS_SDI	AJ34	U32	Y11	AA26	
104	DEBUG(5)	AN23/AM22	AB28/AA26	AG2	AD32	
105	QOFFS_CK	AC27	U25	AH2	H33	
107	QOFFS_LD	AD27	V25	AE18	H32	
122	DAC_Q(13)	AH32	W32	V9	Y32	
124	DAC_Q(12)	AH33	V32	V8	Y31	
126	DAC_Q(11)	AM32	Y29	Y7	AB28	
128	DAC_Q(10)	AM33	W29	Y8	AB27	
130	DAC_Q(9)	AL33	AA33	AA6	AA31	
132	DAC_Q(8)	AL34	AA34	AA5	AA30	
134	DAC_Q(7)	AH30	Y28	AC5	Y27	
136	DAC_Q(6)	AJ30	Y27	AB6	AA28	
138	DAC_Q(5)	AN27	AH34	AE6	AE33	
140	DAC_Q(4)	AP27	AJ34	AF5	AF33	
142	DAC_Q(3)	AJ29	AA29	AG6	AC29	
144	DAC_Q(2)	AK29	AA28	AF6	AC30	
146	DAC_Q(1)	AF26	AB30	W1	AF31	
148	DAC_Q(0)	AE26	AA30	V2	AG31	
149	DACI_CLK	AK22	AG32	V4	AF36	
150	DACQ_CLK	AN30	AC30	AH5	AJ35	
154	DAC_I(13)	AE27	Y24	Y1	AD27	
156	DAC_I(12)	AF28	W24	W2	AC28	
158	DAC_I(11)	AL30	AD32	AA3	AF28	
160	DAC_I(10)	AM30	AE32	AB3	AG28	
162	DAC_I(9)	AH27	AE31	AD2	AG32	
164	DAC_I(8)	AJ27	AF31	AE2	AG33	
166	DAC_I(7)	AL29	AF34	AE3	AN34	
168	DAC_I(6)	AL28	AF33	AF3	AN35	
170	DAC_I(5)	AN24	AB23	AH3	AK32	
172	DAC_I(4)	AP24	AB22	AG3	AK33	
174	DAC_I(3)	AK26	AK34	AP2	AN33	
176	DAC_I(2)	AL26	AK33	AN2	AM33	
178	DAC_I(1)	AM23	AL31	AN3	AG30	
180	DAC_I(0)	AL23	AM31	AM3	AF30	

7.3. Virtex 5

Samtec Pin No.	UCF Name	V5LX	5T1	5T2	Comments
1	SYNTHSEL(3)	AL6	AP14	Y34	
3	SYNTHSEL(2)	AL5	AN14	AA34	
6	TRIG_IO	AP5	AA8	K40	
9	SYNTHSEL(1)	AM6	AB8	P37	
10	TRIG_DIRN	AM7	AM11	U38	
11	SYNTHSEL(0)	AN7	AC8	R37	
13	SYNTH_OE	AN8	AC9	N38	
14	AUX_IO	AL10	AL10	W37	
20	AUX_DIRN	AM11	AJ11	M39	
24	SYNTHREFCK	AP16	AJ9	V39	
26	DEBUG(0)	AM15	AH9	M38	
28	DEBUG(1)	AM16	AH10	L39	
38	DEBUG(2)	AP9	AD10	H40	
40	DEBUG(3)	AP10	AD11	J40	
89	EXTCK_P	AE8	AG5	Y39	was DEBUG(6), rev2 boards
90	IOFFS_SDI	AH9	AH7	T40	
91	EXTCK_N	AF8	AF5	Y38	was SYNTHCK, rev2 boards
92	IOFFS_CK	W7	D11	AF40	
94	IOFFS_LD	AE4	M8	AL42	
97	DEBUG(6)	AA4	K8	AE40	was EXTCK_P, rev2 boards
99	SYNTHCK	AB5	K9	AD40	was EXTCK_N, rev2 boards
102	DEBUG(4)	AG1	T8	AV40	
103	QOFFS_SDI	Y11	E9	AC40	
104	DEBUG(5)	AG2	U7	AU39	
105	QOFFS_CK	AH2	R11	AK38	
107	QOFFS_LD	AE18	H19	K30	
122	DAC_Q(13)	V9	G8	AC41	
124	DAC_Q(12)	V8	H8	AD42	
126	DAC_Q(11)	Y7	D12	AB39	
128	DAC_Q(10)	Y8	C12	AC38	
130	DAC_Q(9)	AA6	A13	AE42	
132	DAC_Q(8)	AA5	B12	AD41	
134	DAC_Q(7)	AC5	C13	AH41	
136	DAC_Q(6)	AB6	B13	AG42	
138	DAC_Q(5)	AE6	E11	AF42	
140	DAC_Q(4)	AF5	F11	AF41	
142	DAC_Q(3)	AG6	E13	AB38	
144	DAC_Q(2)	AF6	E12	AB37	
146	DAC_Q(1)	W1	N8	AE39	
148	DAC_Q(0)	V2	N7	AE38	
149	DACI_CLK	V4	M6	AN39	
150	DACQ_CLK	AH5	G13	AJ40	
154	DAC_I(13)	Y1	P5	AG38	
156	DAC_I(12)	W2	N5	AF39	
158	DAC_I(11)	AA3	K6	AM38	
160	DAC_I(10)	AB3	K7	AN38	
162	DAC_I(9)	AD2	J5	AH38	
164	DAC_I(8)	AE2	J6	AJ37	
166	DAC_I(7)	AE3	J7	AM39	
168	DAC_I(6)	AF3	H7	AL39	
170	DAC_I(5)	AH3	F6	AK39	
172	DAC_I(4)	AG3	F5	AJ38	
174	DAC_I(3)	AP2	G7	AP40	
176	DAC_I(2)	AN2	G6	AN40	
178	DAC_I(1)	AN3	E7	AT40	
180	DAC_I(0)	AM3	E6	AR40	

7.4. Signal Description

7.4.1. Signal DACs

DAC_I(13:0) - High speed dac for the I channel, SMA J2 (DAC 5672)
DACI_CLK - FPGA -supplied data clock for I channel DAC. Max 275 MHz
DAC_Q(13:0)- High speed dac for the Q channel, SMA J1 (DAC 5672)
DACQ_CLK - FPGA -supplied data clock for Q channel DAC. Max 275 MHz

7.4.2. Offset DACs

ON the DC-coupled version of the board, each channel has the ability to vary the DC offset of the signal at the SMA using a pair of 16-bit DACS (one for positive offsets, one for negative offsets) on each channel. Each pair of offset DACs is controlled by an SPI-compatible 3-wire interface. The example application code shows how to use these DACs.

QOFFS_CK - serial interface clock for the Q channel offset DAC (LTC2602)
QOFFS_LD - serial interface load for the Q channel offset DAC (LTC2602)
QOFFS_SDI - serial data in/out for the Q channel offset DAC (LTC2602)

IOFFS_CK - serial interface clock for the Q channel offset DAC (LTC2602)
IOFFS_LD - serial interface load for the I channel offset DAC (LTC2602)
IOFFS_SDI - serial data in/out for the I channel offset DAC (LTC2602)

7.4.3. IO Ports

TRIGIO - FPGA input/output pin connected via IO buffer to SMA J9
TRIG_DIRN - FPGA controlled direction pin for the TRIG port. 1= output, 0= input (default)
AUXIO - FPGA input/output pin connected via IO buffer to SMA J8
AUX_DIRN - FPGA controlled direction pin for the AUX port. 1= output, 0= input (default)

7.4.4. Clock Input

EXTCK_P,EXTCK_N - single-ended drive on J3 is converted to a differential LVDS clock driving these global clock pins on the FPGA.

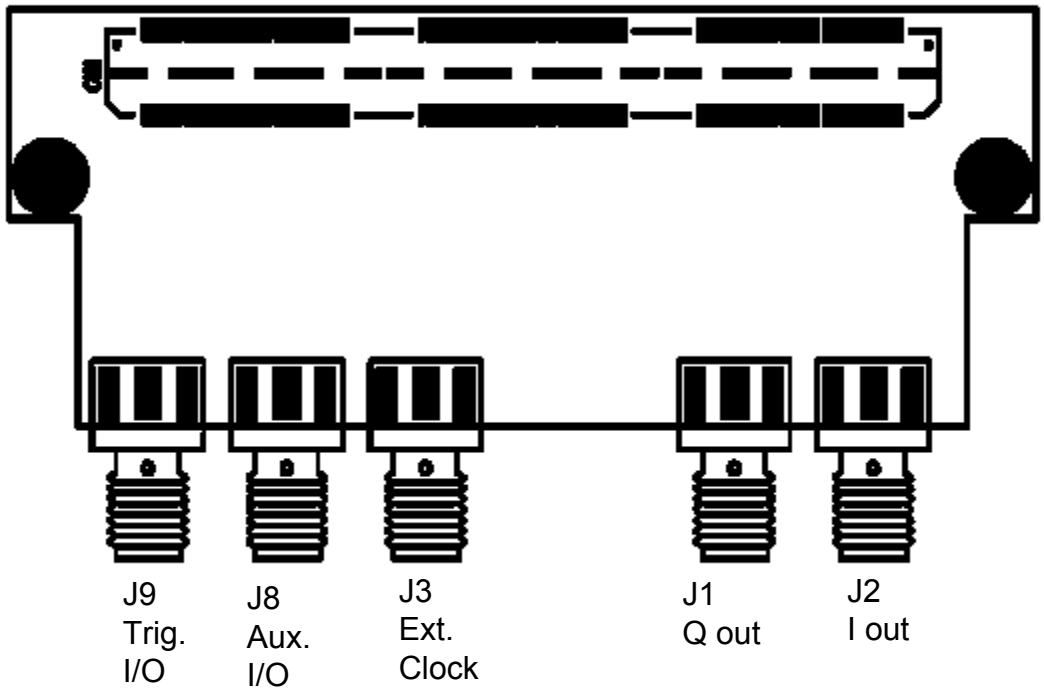
7.4.5. Synth

The board has an ICS-6101M-02 synthesiser built in which allows generation of the sample clock from an external reference (10 MHz to 27MHz). Multiply ratios are >=3, <=16 and the maximum output clock is 170MHz.
SYNTHREFCK - Synthesiser clock input, driven by FPGA pin
SYNTHCK - synthesised clock output driving FPGA global clock input.
SYNTHSEL(3:0) - synthesiser divider ratio control
SYNTH_OE - output enable for synthesised clock

7.4.6. Misc

DEBUG(6:0) - general purpose debug I/O pins connected to pads accessible externally. DEBUG(0) is also connected to 'UFL' style connector J4. Similarly DEBUG(1) is connected to J6, DEBUG(2) to J5 and DEBUG(3) to J7 to provide additional routeing for triggering/synchronisation signals between DAC boards.

Board Layout



Revision History

Date	Revision	Nature of Change
Nov-2006	Draft	First draft
July-2007	1.1	Added photograph
July-2007	1.2	Board name changed, minor typos.
Aug-2007	1.3	Corrected version info and output range.
Sep-2007	1.4	Added signal descriptions.
April-2009	1.5	Added 5T1, 5T2 pins, corrected block diagram
June-2009	1.6	Added AC coupling spec and SFDR figures