XRM-FCN-C1

High Speed Serial Adaptor Module plus Dual JPEG 2000 CODEC

User Guide

Version 1.0

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EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications

Caution

This equipment uses Class 1 Laser devices; such devices are not considered to be hazardous when used for their intended purpose. Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous laser light exposure.

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1. Introduction

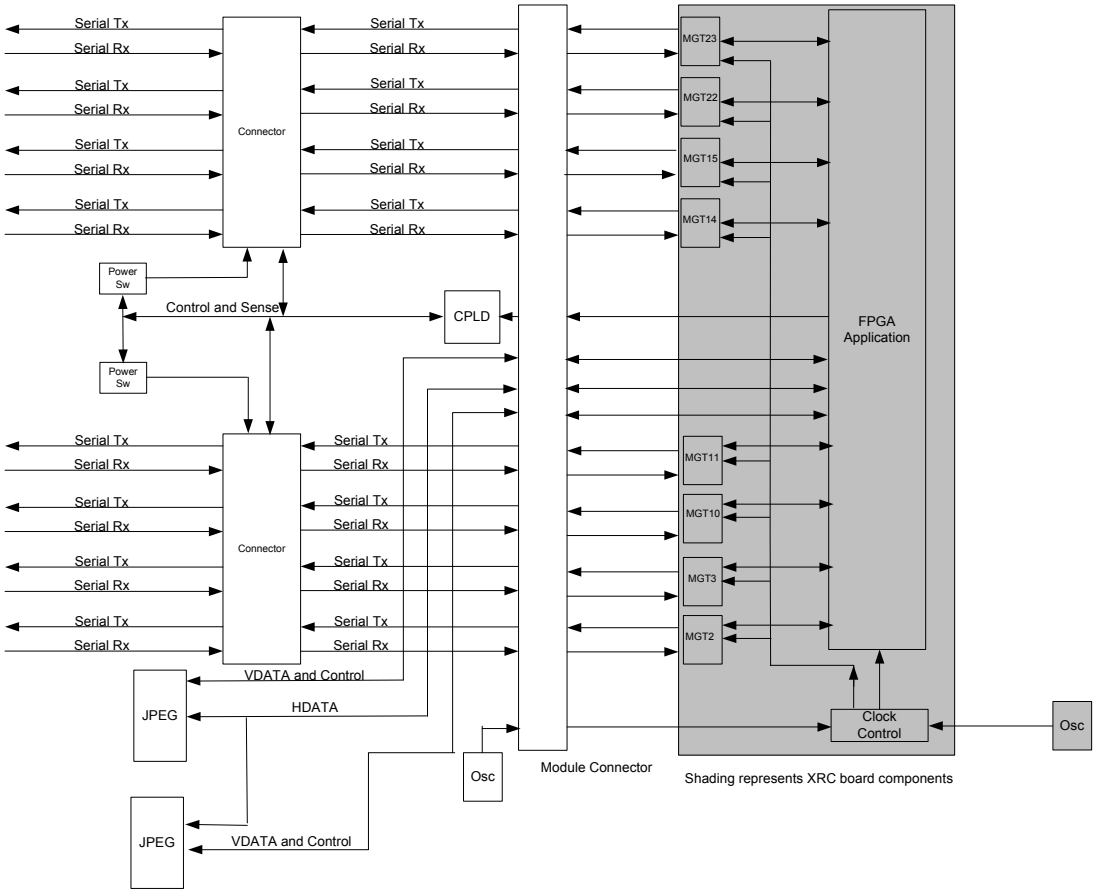
The XRM-FCN-C1 is a front-panel adapter card which provides 8 full duplex channels of high speed serial communications and provides a cost-effective solution to applications requiring high-speed data communications such as Infiniband TA, 10G Ethernet, 4x Fibre Channel and others.

The XRM-FCN-C1 allows easy connection of these cards to devices with compatible connectors and signalling standards by means of simple, point-to-point connection schemes implemented using off-the-shelf cable assemblies. Both copper and optical ('CX4') versions of the FCN connector are supported, with full control and fault signalling for each of the optical power connections.

It is primarily designed for use with Alpha Data's Virtex4FX and Virtex5T PMC cards but can also be used with Alpha Data's Virtex2Pro cards with some reduction in performance.

A separate low-jitter oscillator is provided to support high-bit rate applications where the internal clock is unsuitable.

This board also incorporates a pair of JPEG2000 codecs (Analog Devices ADV212) which can be operated in tandem or separately to provide compression /decompression of video data.



2. Installation

2.1. Fitting

The XRM-FCN-C1 is designed to plug in to the front panel connector (SAMTEC QSH series) on XRC4FX, XRC5 cards. The retaining screws should be tightened to secure the XRM-FCN-C1.

Note: This operation should not be performed while the PMC card is powered up.

2.2. Configuration

The use of these boards with optical modules requires that the FPGA cards be factory-configured to suit. Consult the factory before attempting to use optical modules with FPGA boards that have not been so configured.

2.3. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

2.4. Voltage Settings

This board is a 3V3 only module; users should ensure that the VIO setting on the FPGA card is set to suit this value to ensure no damage can occur.

3. Specification

3.1. Mating Cables

3.1.1. Copper

Suitable cables are available from the Fujitsu “microGiGaCN Cable I/O” range of 8-pair cables in a variety of lengths and styles e.g. FCD-ZZ00001.

Molex provide an alternative source with their ‘LaneLink’ cables e.g. 74526 - 1002

3.1.2. Optical

The optical interface uses external modules which plug in to the standard FCN style connector. These modules (e.g. EMCORE QTR3432) convert the electrical signals to optical format. Inter-module connection uses MJ3MM12RPR-10-0 (available from Fiberconnections Inc.) or similar
Please note that these items are not normally supplied by Alpha Data.

3.2. Ordering Information

The oscillator frequencies can be customised to suit applications requiring specific baud rates. Contact the factory for details.

3.3. Example Applications

Dual Infiniband 4x (4 lanes at 2.5Gb/s over copper or optical fibre)
Dual 10Gb/s Ethernet CX4 (4 lanes at 3.125Gb/s over copper or optical fibre)
Dual 10Gb/s FibreChannel (4 lanes at 3.1875Gb/s over copper or optical fibre)
Dual 4 x OC-48 SONET

4. Related Documents

ADM-XRC4FX User Manual
ADM-XRC5T1 User Manual
ADM-XRC5T2 User Manual

Infiniband™ Architecture Specification, Volume 2

ADV212 Data Sheet and associated files

5. Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

5.1. Important Note

Optical modules provide a signal ('sense_l') indicating that they are present; however the presence of optical modules cannot be distinguished from a copper connection by relying on this signal alone.

Whilst the optical module supplies are disabled by default and protected by current limiting, the method shown in the example code should always be used to ensure that supplies do not drive into the short circuit presented when a copper cable is fitted.

Designers should ensure that the CPLD code instantiates a pull-up for the 'fault' and 'op_disable' pins. Power to the modules should then only be enabled when the 'sense_l' line is low **and** 'fault' is high.

Pulling 'op_disable' high ensure no inadvertent emission of radiation.

The 'over_current_l' signal from the supplies are open-collector outputs and should also have a pullup instantiated in the CPLD.

6. Pinouts

6.1. High-Speed Serial Link

Signal Name	Pin No	XRC2Pro	XRC4FX	XRC5T1	XRC5T2
txp<0>	DP-1	A40	A36	U2	AA2
txn<0>	DP-3	A41	A37	T2	Y2
rxp<0>	DP-2	A39	C39	T1	Y1
rxn<0>	DP-4	A38	D39	R1	W1
txp<1>	DP-5	A36	A34	M2	T2
txn<1>	DP-7	A37	A35	N2	U2
rxp<1>	DP-6	A35	A31	N1	U1
rxn<1>	DP-8	A34	A32	P1	V1
txp<2>	DP-17	BB4	P39	L2	R2
txn<2>	DP-19	BB5	R39	K2	P2
rxp<2>	DP-18	BB3	U39	K1	P1
rxn<2>	DP-20	BB2	V39	J1	N1
txp<3>	DP-21	BB8	M39	F2	K2
txn<3>	DP-23	BB9	Ne9	G2	L2
rxp<3>	DP-22	BB7	J39	G1	L1
rxn<3>	DP-24	BB6	K39	H1	M1
txp<4>	DP-9	A8	AT39	E2	J2
txn<4>	DP-11	A9	AU39	D2	H2
rxp<4>	DP-10	A7	AW37	D1	H1
rxn<4>	DP-12	A6	AW36	C1	G1
txp<5>	DP-13	A4	AP39	B4	D2
txn<5>	DP-15	A5	AR39	B3	E2
rxp<5>	DP-14	A3	AL39	A3	E1
rxn<5>	DP-16	A2	AM39	A2	F1
txp<6>	DP-25	BB36	AW25	B5	B1
txn<6>	DP-27	BB37	AW24	B6	B2
rxp<6>	DP-26	BB35	AW22	A6	A2
rxn<6>	DP-28	BB34	AW21	A7	A3
txp<7>	XRM-117	BB40	AW28	B10	B6
txn<7>	XRM-119	BB41	AW27	B9	B5
rxp<7>	XRM-118	BB39	AW31	A9	A5
rxn<7>	XRM-120	BB38	AW30	A8	A4

Notes

1) The on-board oscillator can be used to drive a pair of dedicated reference clock pins (mgt_refck_p, mgt_refck_n in the UCF) for the MGTs.
2) Pin numbering and allocation in accordance with Infiniband™ Architecture Specification, Volume 2 section 7.4.3. (Release 1.2)
3) DP= Samtec 28 way differential pair connector. XRM= main Samtec connector

6.2. JPEG Processor Interface

Signal Name	Pin No.	XP	XRC4FX	XRC5T1	XRC5T2
addr<0>	78	K16	D36	W9	K42
addr<1>	81	K19	K34	AJ6	Y42
addr<2>	76	M16	E34	V7	W41
addr<3>	74	L16	F34	W7	V40
mclk_cn1	23	H12	D30	AK8	E39
a_ack_l	2	C13	L28	AA10	J38
a_cs_l	3	E10	C28	AN14	AA34
a_dack_l<0>	6	H13	J29	AA8	K40
a_dack_l<1>	7	E11	K29	AN13	Y35
a_dreq_l<0>	8	G13	H29	AA9	K39
a_dreq_l<1>	10	M19	F29	AM11	U38
a_irq_l	4	D13	K28	AB10	K38
a_rd_l	1	D10	C27	AP14	Y34
a_we_l	5	F11	L29	AM13	W35
b_ack_l	83	J19	L34	AJ7	W42
b_cs_l	75	G18	E37	AE7	W40
b_dack_l<0>	82	H16	J37	V8	AA40
b_dack_l<1>	84	G16	J36	U8	AA39
b_dreq_l<0>	86	M17	M32	V9	P40
b_dreq_l<1>	103	G27	N33	E9	AC40
b_irq_l	77	E17	G36	Y11	U42
b_rd_l	80	J16	E36	W10	J42
b_we_l	79	E18	F36	W11	V41
hdat<0>	98	C29	G37	F8	AB42
hdat<1>	89	K21	E32/M28	AG5	Y39
hdat<2>	15	F10	G27	AC10	P38
hdat<3>	19	H9	F30	AD9	G39
hdat<4>	28	J13	E26	AH10	L39
hdat<5>	40	G21	D25/F24	AD11	J40
hdat<6>	17	G9	G30	AE8	G38
hdat<7>	32	C10	L30	AG11	AA36
hdat<8>	26	K13	D26	AH9	M38
hdat<9>	36	G12	F33	AB6	F42
hdat<10>	13	G10	H27	AC9	N38
hdat<11>	20	F13	K26	AJ11	M39
hdat<12>	34	F12	E33	AB7	G42
hdat<13>	38	F21	C25/F25	AD10	H40
hdat<14>	11	H10	E28	AC8	R37
hdat<15>	22	E9	G26	AJ10	W38
hdat<16>	24	F9	F26	AJ9	V39
hdat<17>	16	K18	J30	AL11	W36
hdat<18>	30	C11	L31	AG10	AA35
hdat<19>	33	G17	G32	AC5	G41
hdat<20>	72	C14	G35	W6	H41
hdat<21>	70	C15	F35	Y6	J41

hdat<22>	73	H18	D37	AF6	Y40
hdat<23>	64	J20	C33	AC7	Y37
hdat<24>	71	H17	D34	AD6	P41
hdat<25>	66	F15	J32	Y7	M41
hdat<26>	68	E15	K32	AA6	L42
hdat<27>	69	J17	C34	AE6	R40
hdat<28>	67	L17	C24	AD4	T42
hdat<29>	63	C20	D24	AA5	M42
hdat<30>	65	K17	C23	AD5	U41
hdat<31>	61	D20	E24	AB5	N41
vclk_cn1	85	H19	M31	AK6	AA41
field	87	G19	N30	AK7	AA42
hsync	88	M18	N32	V10	N40
vsync	91	J21	D32/M27	AF5	Y38
a_vdat<0>	62	H20	C32	AD7	AA37
a_vdat<1>	31	K12	E31	AG8	H38
a_vdat<2>	27	L13	G31	AF11	F39
a_vdat<3>	37	L13	G28	AP12	R39
a_vdat<4>	35	F17	G33	AC4	F41
a_vdat<5>	25	M13	F31	AE11	F40
a_vdat<6>	12	L19	E29	AM12	T37
a_vdat<7>	29	L12	D31	AH8	H39
a_vdat<8>	21	J12	C30	AK9	E40
a_vdat<9>	14	L18	H30	AL10	W37
a_vdat<10>	9	J10	F28	AB8	P37
a_vdat<11>	18	E13	J26	AK11	N39
b_vdat<0>	96	F28	M36	L4	AE37
b_vdat<1>	102	J22	V37/V35	T8	AV40
b_vdat<2>	104	K22	U37/U35	U7	AU39
b_vdat<3>	100	C28	H37	F9	AB41
b_vdat<4>	101	H27	M33	E8	AC39
b_vdat<5>	99	F22	T34/T36	K9	AD40
b_vdat<6>	93	E19	D27	AF9	T39
b_vdat<7>	92	D19	N35	D11	AF40
b_vdat<8>	94	E28	N34	M8	AL42
b_vdat<9>	97	G22	T35/U36	K8	AE40
b_vdat<10>	90	C19	L26	AH7	T40
b_vdat<11>	95	F19	G25	Y8	L40

6.2.1. Signal Description

See the ADV212 data sheet and associated literature for a full description of the operation of these pins.

Common to both processors

addr<1> to <3> -ADV212 address bus
mclk_cn1 - ADV212 system clock
hdat<0> to <31> -ADV212 host data bus
field -ADV212 field sync for video mode

hsync -ADV212 horizontal sync for video mode
vsync -ADV212 vertical sync for video mode

Processor A only
a_ack_l -ADV212 acknowledge signal
a_cs_l - ADV212 chip select signal
a_dack_l<0> to <1>- ADV212 DMA acknowledge signals
a_dreq_l<0> to <1>- ADV212 DMA request signals
a_irq_l - ADV212 interrupt request signal
a_rd_l - ADV212 read enable for host interface operation
a_we_l - ADV212 write enable for host interface operation
a_vdat<0> to <11> -ADV212 video data bus

Processor B only
b_ack_l -ADV212 acknowledge signal
b_cs_l - ADV212 chip select signal
b_dack_l<0> to <1>- ADV212 DMA acknowledge signals
b_dreq_l<0> to <1>- ADV212 DMA request signals
b_irq_l - ADV212 interrupt request signal
b_rd_l - ADV212 read enable for host interface operation
b_we_l - ADV212 write enable for host interface operation
b_vdat<0> to <11> -ADV212 video data bus

6.3. CPLD Interface

Signal Name	Pin No	XP	XRC4FX	XRC5T1	XRC5T2
cpld_data	105	J27	J27	R11	AK38
cpld_dclock	106	L27	AC25	H20	L30
cpld_reset	107	K27	K27	H19	K30

cpld_data - serial i/o data for optical module power and control functions
cpld_dclock - clock for serial i/o transactions
cpld_reset - reset line to ensure safe state when FPGA unconfigured

6.3.1. CPLD Signals

The CPLD is used to provide control of the following signals via the serial link.

Link Control
BREFCK_ENAB -high to enable the oscillator on the XRM
STATUS_1 -Infiniband STATUS led (yellow) connector 1
ATTEN_1 -Infiniband ATTEN led (green) connector 1
STATUS_2 -Infiniband STATUS led (yellow) connector 2
ATTEN_2 -Infiniband ATTEN led (green) connector 2

Opto Power
PSUEN1 -high to enable the opto supply for connector 1
PSUEN2 -high to enable the opto supply for connector 2

OC_L1	-low to signal overcurrent, opto supply for connector 1
OC_L2	-low to signal overcurrent, opto supply for connector 2

Opto Control

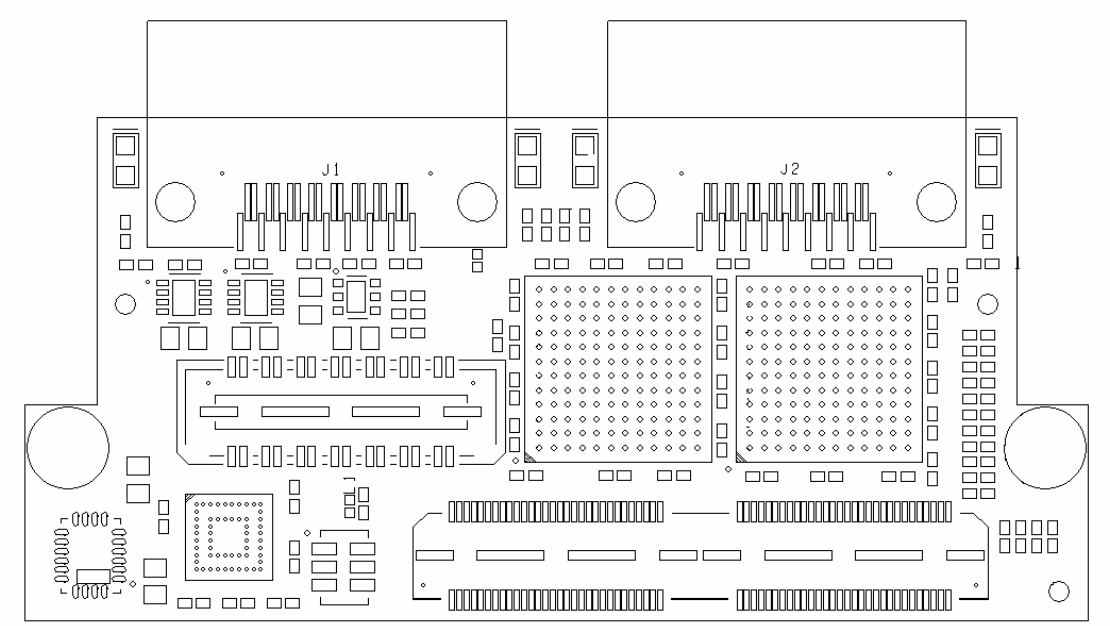
SENSE1	-low to indicate that an opto module has been fitted to connector 1
FAULT1	-low to indicate that no data detected on the opto Rx channel, connector 1
SENSE2	-low to indicate that an opto module has been fitted to connector 2
FAULT2	-low to indicate that no data detected on the opto Rx channel, connector 2
ODIS1	-low when CPLD Reset is asserted to disable Tx on any module fitted
ODIS2	-low when CPLD Reset is asserted to disable Tx on any module fitted

ADV212 Control

JPEG_RESET_L	-asynchronous processor reset for ADV212's
SCOM5	-synchronisation signal for multi-chip operation

CPLD programming is implemented by means of the JTAG chain on the FPGA card.

Board Layout



Revision History

Date	Revision	Nature of Change
Feb-2008	-	Initial draft