ALPHA DATA

XRM-RS485
User Manual

Revision: V1.2.1

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1 Introduction

The XRM-RS485 is an I/O module for the ADM-XRC series of FPGA cards.

The XRM-RS485 provides 19 RS485 half-duplex channels. Each link can operate in transmit or receive mode. The FPGA board, through the XRM connector has control over the transmit and receive data, transmit enable and termination enable of each channel.

In addition, the board provides two auxiliary I/O connections on 50Ω MCX connectors. These provide input /output signalling at 3.3V or 5V.

1.1 Specifications

The XRM-RS485 provides multiple channels of bidirectional RS485 capability with complete programmability.

- Standard XRM format module
- Compatible with ADM-XRC-II, ADM-XP, ADM-XRC-4 and ADM-XRC5 series
- 19 Independent RS485 channels
- 2 Aux LVTTL/TTL
- Bidirectional capability with programmable termination
- RS422 compatible with programmable transmit/receive configuration
- High speed of 20Mbaud using LTC2854 transceivers
- XRM VCCIO of 1.8V, 2.5V or 3.3V

1.2 Block Diagram

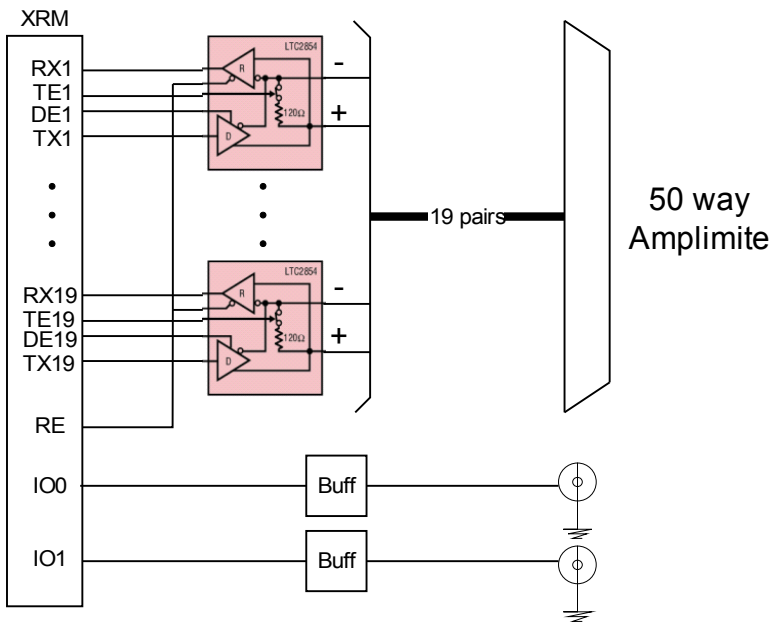

Figure 1 : XRM-RS485 Block Diagram

2 Installation

2.1 Fitting

The XRM-RS485 is designed to plug in to the front panel connector (SAMTEC QSH series) on ADM-XRC-II, II-PRO, XRC-4LX/SX/FX, all XRC-5 cards and all XRC6 cards. The retaining screws should be tightened to secure the XRM-RS485.

Note:
This operation should not be performed while the PMC card is powered up.

2.2 Configuration

The use of these boards with optical modules requires that the FPGA cards be factory-configured to suit. Consult the factory before attempting to use optical modules with FPGA boards that have not been so configured.

2.3 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.

Avoid flexing the board.

2.4 Voltage Settings

This board employs level translators to support the full range of possible VIO settings on the FPGA card. For XRC6 boards, this voltage is set automatically to 2.5V.

3 Hardware Description

Please refer to the SDK installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

4 XRM Interface - Standard Signals and Power

The XRM-RS485 can use 3.3V, 2.5V or 1.8V signalling voltages. On XRC6 boards, this voltage is set automatically to 2.5V

The operation of each RS485 transceiver is controlled by the FPGA signals RE_L, DE, TE, T and R. Additionally, the bidirectional line side differential pair is wired directly to the interface connector, J1. For details of the transceiver, refer to the data sheet for the Linear Technology LTC2854. All transceivers have individual controls except for RE_L which is common to all devices and which provides some protection against contention. The key to these signal names is show in Table 1 - "XRM Signal Key".

Signal	Function	Driven By	Comments
RE_L (pin 81)	Receive Enable - active low	FPGA Card	Pulled low on the XRM (10kΩ)
DE [1 to 19]	Drive Enable - active high	FPGA Card	Pulled low on the XRM (10kΩ)
TE [1 to 19]	Termination enable - active high	FPGA Card	Drive high to enable differential termination on line side.
T [1 to 19]	Transmit Data	FPGA Card	
R [1 to 19]	Receive Data	XRM-RS485	Enabled by RE_L=0, otherwise looped back Tx data.
RSRVD	Reserved function	N/A	Factory use only.

Table 1 : XRM Signal Key

The auxiliary I/O connections, XRM_NI_SYNC (J2) and XRM_NI_CLOCK (J3), are configured using 0R resistors to provide either LVTTL (3.3V) or TTL (5.0V) signalling via the MCX connectors.

XRM_NI_SYNC is configured as an output (FPGA to MCX) by setting XRM_SYNC_DIRN high and as an input (MCX to FPGA, default) by setting XRM_SYNC_DIRN low .

XRM_NI_CLOCK is configured as an output (FPGA to MCX) by setting XRM_CLOCK_DIRN high and as an input (MCX to FPGA, default) by setting XRM_CLOCK_DIRN low .

XRM_OE is a global enable for the level translators and should normally be driven high when the FPGA is configured.

The XRM interface is implemented on CN1, a 120 pin Samtec connector type QTH, with the pin-out as detailed in tables Table 2 - "XRM Interface - part 1" to Table 3 - "XRM Interface - part 2".

Signal	Samtec Pin	Samtec Pin	Signal
TE2	1	2	R9
T2	3	4	R7
TE1	5	6	R5
T1	7	8	R3
DE2	9	10	R4
DE1	11	12	R8
TE3	13	14	R11
T3	15	16	R2
DE3	17	18	R1
TE5	19	20	R10
T5	21	22	R12
DE5	23	24	R14
XRM_NI_SYNC	25	26	R13
TE4	27	28	R15
T4	29	30	R16
DE4	31	32	R6
TE6	33	34	R18
T6	35	36	R19
DE6	37	38	R17
RSRVD	39	40	XRM_NI_CLK
RSRVD	41	42	RSRVD
RSRVD	43	44	N.C.
N.C.	45	46	N.C.
N.C.	47	48	N.C.
RSRVD	49	50	N.C.
N.C.	51	52	N.C.
N.C.	53	54	N.C.
RSRVD	55	56	RSRVD
N.C.	57	58	N.C.
N.C.	59	60	RSRVD

Table 2 : XRM Interface - part 1

Signal	Samtec Pin	Samtec Pin	Signal
TE7	61	62	DE8
T7	63	64	T8
DE7	65	66	TE8
TE9	67	68	TE11
DE9	69	70	T11
T9	71	72	DE11
TE15	73	74	TE13
T15	75	76	T13
DE15	77	78	DE13
N.C.	79	80	TE10
RE_L	81	82	T10
N.C.	83	84	DE10
N.C.	85	86	XRM_SYNC_DIRN.
N.C.	87	88	XRM_CLOCK_DIRN
XRM_OE	89	90	TE17
TE18	91	92	T17
T18	93	94	DE17
DE18	95	96	DE14
TE16	97	98	T14
T16	99	100	TE14
DE16	101	102	DE12
TE19	103	104	TE12
T19	105	106	T12
DE19	107	108	N.C.
N.C.	109	110	N.C.
N.C.	111	112	N.C.
N.C.	113	114	N.C.
N.C.	115	116	N.C.
N.C.	117	118	N.C.
N.C.	119	120	N.C.

Table 3 : XRM Interface - part 2

5 RS485 Interface Connector

The RS485 signal interface is a SCSI style 50 way female connector, AMP part number 787394-5 (or it's RoHS equivalent).

The pin out is as shown below in Figure 2 - "RS485 Interface Connector".

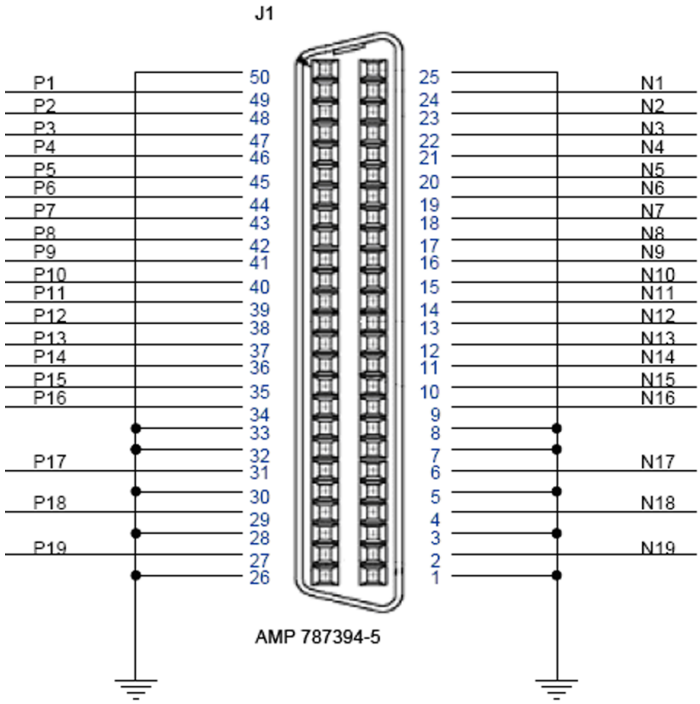

Figure 2 : RS485 Interface Connector

Revision History

Date	Revision	Nature of Change
July 2008	1.0	Initial Release issue
December 2010	1.1	Corrected signal polarity.Updated block diagram. Converted User Guide to XML.
January 2013	1.2	Corrected 'RE' signal polarity.Updated supported boards
January 2013	1.2.1	Corrected signal polarity in XRM-RS485 Block Diagram.

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