



## IF/Baseband Signal Sampling

## Board Features

- Dual 12-bit 500Mps ADCs
- External Clock Input

## Summary

The **XRM2-ADC-D7/500** is an XRM2 I/O Module, providing two Analog to Digital converters with 12-bit resolution and sampling rates up to 500Mps.

Aimed at IF/Baseband Signal Sampling, the sampling clock can be sourced from either an external clock source or from a clock generated within the attached FPGA board. A Trigger I/O port is provided for use as a trigger control and an Auxiliary I/O port for general purpose signaling. An additional two ports are available for use as high-speed interconnect between boards for synchronisation.

## Deliverables

XRM2-ADC-D7/500 Board  
 One Year Warranty  
 One Year Technical Support

## Input/Output Interfaces

### 2x Dual Analog to Digital Converters

Resolution: 12-bit  
 Max Sample Freq: 500Mps  
 Bandwidth: 4.5 MHz to 700 MHz (3 dB)  
 Impedance: 50Ω  
 Connector: SMA

### 1x External Clock Input

Impedance: 50Ω - AC coupled  
 Levels: 0 dBm (640 mV pk to pk) to +12 dBm maximum (2.5 V pk to pk) nominal  
 Connector: SMA

### 1x Trigger I/O

Impedance: 4k7Ω (DC coupled)  
 Levels: +3V3 LVTTTL  
 Connector: SMA

### 1x Auxiliary I/O

Impedance: 4k7Ω (DC coupled)  
 Levels: +3V3 LVTTTL  
 Connector: SMA



**Support**

Example UCF, HDL files and Application software are provided with the board.

**Environmental Specification****Temperature Ranges**

Cooling Option	Operating Temperatures		Storage Temperatures	
	Min	Max	Min	Max
AC0	0°C	55°C	-40°C	85°C

Operating Humidity : Up to 95% (non-condensing)

**EMC Standards**

FCC 47CFR Part 2

EN55022:2010 Equipment ClassB

**Ordering Information****Order Code: XRM2-ADC-D7/500**

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