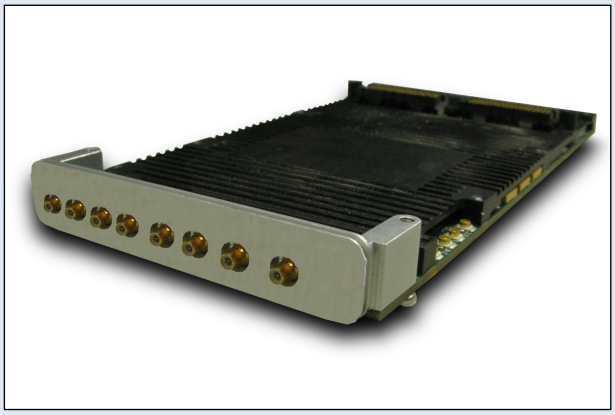
ADM-XRC-6T-DA1

ALPHA DATA

10th September 2014 **Datasheet Revision: 1.0**



Summary

The **ADM-XRC-6T-DA1** is a high performance reconfigurable XMC (Switching Mezzanine Card) based on the Xilinx™ Virtex-6 LXT and SXT range of Platform FPGAs. It Provides onboard Analog to Digital and Digital to Analog functionality for data sampling/generation.

Features include high speed PCI Express® interface, external memory, Analog I/O, high density I/O, programmable clocks, temperature monitoring and flash boot facilities.
A comprehensive cross platform API with support for **Microsoft Windows™**, **Linux** and **VxWorks** provides access to the full functionality of these hardware features.

Features

Applications:

Signal Capture/Generation

Target Devices:

Xilinx Virtex-6: LX240T, LX365T, LX550T, SX315T, SX475T (FFG1759)

Memory:

SDRAM - 1GByte in 4 independent banks (256Mbyte) of DDR-3 SDRAM 64M x 32-bits @ 400MHz

SDRAM - 2GByte in 4 independent banks (512Mbyte) of DDR-3 SDRAM 128M x 32-bits @ 400MHz option

FLASH - 4MByte serial Flash

FLASH - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.

Front Connector I/O:

Single/Dual 12-bit ADC up to 1.8Gsps/3.6Gsps

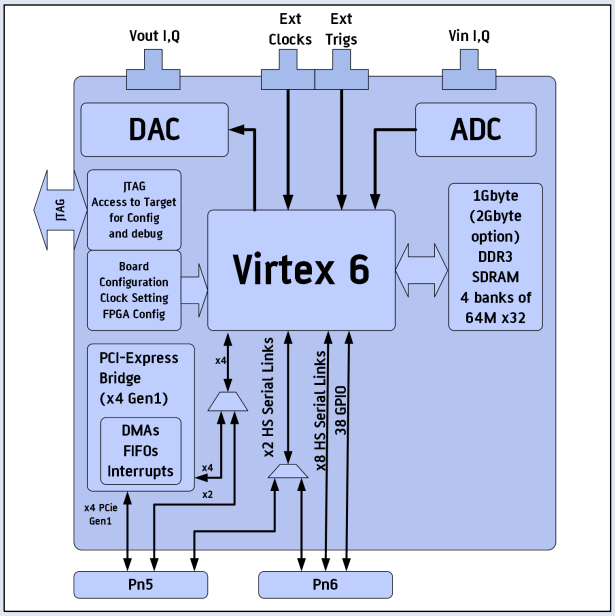
Dual 14-bit DACs up to 2.5GHz

External Clock Inputs

External Trigger Inputs

Rear Connector I/O:

8 High-Speed Serial Links via P15 connector (allowing second x4 PCI Express® channel from Target FPGA)
8 High-Speed Serial Links via P16 connector
38 LVTTL GPIO connections via P16 connector (VITA 46.9 X38S compatible pinout)



ADM-XRC-6T-DA1

Specification	
Product Name	ADM-XRC-6T-DA1
Target Devices	Xilinx Virtex-6 - LX240T, LX365T, LX550T, SX315T, SX475T (FFG1759)
Host I/F	PCI Express®
Interface	PCI Express® Gen1 x4 4 DMA controllers
Memory	**SDRAM** - 1GByte in 4 independent banks (256Mbyte) of DDR-3 SDRAM 64M x 32-bits @ 400MHz **SDRAM** - 2GByte in 4 independent banks (512Mbyte) of DDR-3 SDRAM 128M x 32-bits @ 400MHz option **FLASH** - 4MByte serial Flash **FLASH** - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.
Front I/O	**ADC Inputs:** Single/Dual 12-bit ADC up to 1.8Gsps/3.6Gsps bandwidth = 10MHz to 2400MHz nominal levels = Range1: ±800 mV nominal, Range2: ±1000 mV nominal impedance = 50 Ohms resolution = 12-bit fmax = 3.6GHz **DAC Outputs:** Dual 14-bit DACs up to 2.5GHz resolution = 14-bit bandwidth = 1GHz fmax = 2.5GHz Multi-Nyquist Filtering, Nyquist Zones 1,2,3 selectable **Ext Clock:** External Clock Inputs levels = ±200 mV ppk to ±2V ppk **Ext Trig:** External Trigger Inputs levels = LVTTL
Rear I/O	8 High-Speed Serial Links via P15 connector (allowing second x4 PCI Express® channel from Target FPGA) 8 High-Speed Serial Links via P16 connector 38 LVTTL GPIO connections via P16 connector (VITA 46.9 X38S compatible pinout)
Special Functions	**Dual DAC interface** (14-bit at 2.5GHz) **Software-configurable Single(12 bit at 3.6 GHz) or Dual ADC interface** (12-bit at 1.8GHz)
Clocks	Low-jitter 250MHz reference clock Low-jitter 200MHz reference clock
Device Configuration	PCI Bus direct to SelectMAP port From Flash direct on power up External JTAG connector
Software	Drivers for Microsoft Windows™, Linux and VxWorks API with template designs in VHDL and Verilog
Environmental	**Temperature:** AC1 - air cooled industrial CC1 - conduction cooled industrial **EMC:** FCC 47CFR Part 2 EN55022 Equipment Class B

Ordering Codes		
ADM-XRC-6T-DA1/z-y(c)(m)		
Virtex-6 device	z	LX240T, LX365T, LX550T, SX315T, SX475T
Virtex-6 speed	y	1, 2, 3
Cooling	c	/AC1 = air cooled industrial, /CC1 = conduction cooled industrial
Memory Size Fitted	m	blank =each bank has 256MByte - 1GByte for the card, /1 = each bank has 512MByte - 2GByte for the card
Note	#	Not all FPGA speed grades available in all configurations. Contact Alpha Data for details

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