Features

Applications:

Military, Aerospace, High Performance Computing, Scientific/Instrumentation, Broadcast, Medical/Bioinformatics, Telecoms, Security

Target Devices:

Xilinx Virtex-5 - LX110T, LX155T, LX220T, LX330T, SX240T, FX100T, FX130T, FX200T (FFG1738)

Memory:

SDRAM - 1GByte in 4 independent banks of DDR-II SDRAM
64M x 32-bits @ 333MHz

SSRAM - 4MByte QDR-II SSRAM in 2 independent banks
1M x 18-bits
(compatible with Xilinx™ MIG controllers)
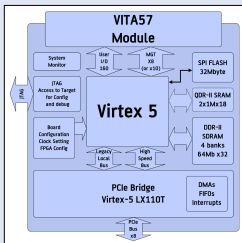Only fitted on boards fitted with LX330T, SX3240T or FX200T.
No SSRAM fitted otherwise.

FLASH - 4MByte serial Flash

FLASH - Configuration Flash providing an initialisation
design for automatic loading into the target FPGA.

Front Connector I/O:

Up to 160 LVTTL/LVDS I/O - Programmable signaling levels
of 2.5V or 3.3V

8 (or 10 - depends on Target FPGA being LX330T or
FX200T) High-Speed Serial Links via a range of FMC
(VITA57) front panel adapters

Summary

The **ADPe-XRC-5T** is a high performance reconfigurable
PCI Express® Card based on the Xilinx Virtex-5 range
of Platform FPGAs. Features include high speed PCIe
interface, **QDR-II SSRAM**, DDR-II SDRAM, **VITA57 FMC
high density I/O**, programmable clocks, temperature
monitoring, battery backed encryption and flash boot
facilities.

A comprehensive cross platform API with support for
Microsoft Windows™, **Linux** and **VxWorks** provides
access to the full functionality of these hardware
features.

Specification

Product Name	ADPe-XRC-5T
Target Devices	Xilinx Virtex-5 - LX110T, LX155T, LX220T, LX330T, SX240T, FX100T, FX130T, FX200T (FFG1738)
Host I/F	PCI Express® x8
Interface	x8 PCI Express®
Memory	**SDRAM** - 1GByte in 4 independent banks of DDR-II SDRAM 64M x 32-bits @ 333MHz **SSRAM** - 4MByte QDR-II SSRAM in 2 independent banks 1M x 18-bits (compatible with Xilinx™ MIG controllers) Only fitted on boards fitted with LX330T, SX240T or FX200T. No SSRAM fitted otherwise. **FLASH** - 4MByte serial Flash **FLASH** - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.
Front I/O	Up to 160 LVTTL/LVDS I/O - Programmable signaling levels of 2.5V or 3.3V8 (or 10 - depends on Target FPGA being LX330T or FX200T) High-Speed Serial Links via a range of FMC (VITA57) front panel adapters
Clocks	Low-jitter user clock, programmable up to 637.5MHz Additional 200MHz reference clock for IOB delay circuits.
Device Configuration	PCI Express® Bus direct to SelectMAP port From Flash direct on power up External JTAG connector
Software	Drivers for Microsoft Windows™, Linux and VxWorks API with template designs in VHDL and Verilog
Battery	Onboard dual battery back-up for IP encryption keys.
Environmental	**Temperature:** **Air cooled option (AC0)** Operating Temperature 0° to +55°C **Air cooled industrial option (AC1)** Operating Temperature -20° to +55°C **EMC:** FCC 47CFR Part 2 EN55022 Equipment Class B

Ordering Codes

ADPe-XRC-5T/z-y(m)(c)	
Virtex-5 device	z	LX110T, LX155T, LX220T, LX330T, SX240T, FX100T, FX130T, FX200T
Virtex-5 Speed	y	1, 2, 3
Memory Upgrade	m	blank=1GBit devices - 256MBytes per bank - 1GBytes for the board, /2=2GBit devices - 512MBytes per bank - 2GBytes for the board
Air cooled	c	blank = air cooled commercial, /AC1 = air cooled industrial