XRM-CLINK-GIGE

CameraLink/GigE Adaptor Module

User Guide

Version 2.0

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EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications

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1. Introduction

Photograph 1 - XRM-CLINK-GIGE

The XRM-CLINK-GIGE provides a 1000/100/10 Ethernet PHY, RS232 transceiver, and mini Cameralink interfaces for the Alpha Data's FPGA based platforms. The XRM-CLINK-GIGE is designed to allow the deployment of systems that require Gigabit Ethernet capability (for example GigE-Cameralink) and mini Cameralink connectivity.

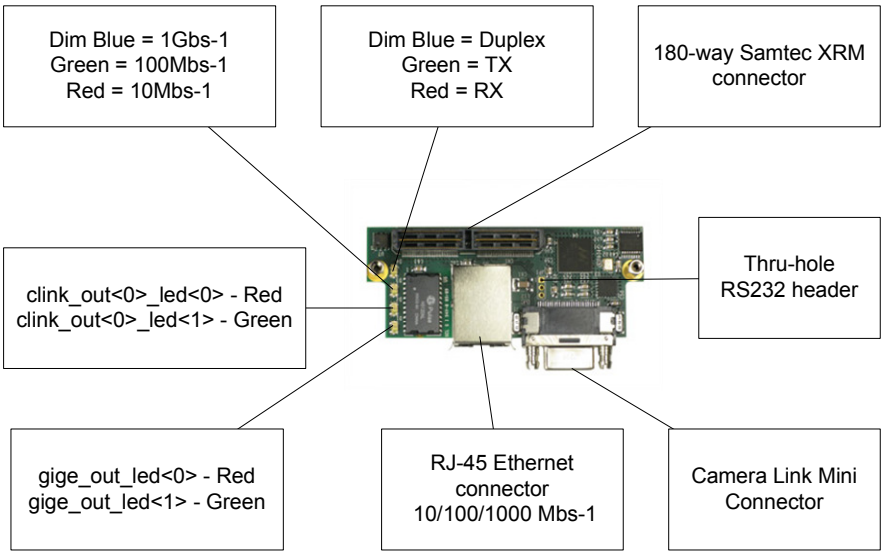

Figure 1 - XRM-CLINK-GIGE features

2. Installation

The XRM-CLINK-GIGE is designed to plug in to the front panel connector (SAMTEC QSH series) on the FPGA base card. The retaining screws should be tightened to secure the XRM-CLINK-GIGE.

Ensure that the VIO voltage for the base FPGA card is set to 2.5V. Please refer to the base FPGA User Guide on setting the VIO voltage.

Note: This operation should not be performed while the FPGA card is powered up.

2.1. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

3. Specification

3.1. Connectors

SDR connector 3M™ part number 12226-8250-00FR
RJ45

3.2. Mating Cableform

SDR cable assembly 3M™ part number 1SF26-L120-00C-XXX,
where XXX= length in centimetres.

SDR to MDR cable assembly 3M™ part number 1MF26-L560-00C-XXX,
where XXX= length in centimetres.

Standard 10/100/1000 CAT5e/CAT6 Ethernet cable

3.3. Misc.

RS232 transceiver controlled from FPGA implementing 3-wire interface.
Connection via 3-pin 1mm thru-hole header.

4. Related Documents

ADM-XRC-5T1 User Manual
Available from Alpha Data

CameraLink Technology Brief
Available from www.baslerweb.com

Marvell 88E1111 1-Port Gigabit Ethernet Transceiver Manual
Available from Marvell with NDA

Xilinx Virtex-5 User Guides
http://www.xilinx.com/support/documentation/virtex-5.htm#19297

Xilinx EDK documentation
http://www.xilinx.com/ise/embedded_design_prod/platform_studio.htm

5. Pinouts

Please refer to the relevant constraints file for the base FPGA card for FPGA pin LOCs found in the ADMXRC_SDK:

<ADMXRC_SDK Install dir>\ucf\<FPGA card>\adm<FPGA card>_samtec.ucf

PHY (Marvell 88E1111)

UCF name	Samtec pin
gige_in_clk125	89
gige_in_col	35
gige_in_crs	27
gige_in_int_l	28
gige_in_pok	32
gige_in_rxClk	40
gige_in_rxData<0>	25
gige_in_rxData<1>	9
gige_in_rxData<2>	21
gige_in_rxData<3>	37
gige_in_rxData<4>	5
gige_in_rxData<5>	1
gige_in_rxData<6>	17
gige_in_rxData<7>	33
gige_in_rxDv	13
gige_in_rxEr	31
gige_in_txClk	38
gige_inout_mdio	24
gige_out_coma	34
gige_out_gtxClk	91
gige_out_mdc	36
gige_out_reset_l	30
gige_out_txData<0>	11
gige_out_txData<1>	19
gige_out_txData<2>	7
gige_out_txData<3>	3
gige_out_txData<4>	4
gige_out_txData<5>	6
gige_out_txData<6>	26
gige_out_txData<7>	2
gige_out_txEn	23
gige_out_txEr	15

LEDs

UCF name	Samtec pin
clink_out<0>_led<0>	14
clink_out<0>_led<1>	16
gige_out_led<0>	71
gige_out_led<1>	69

CameraLink

UCF name	Samtec pin
clink_in<0>_d_n<0><0>	62
clink_in<0>_d_p<0><0>	64
clink_in<0>_d_n<0><1>	66
clink_in<0>_d_p<0><1>	68
clink_in<0>_d_n<0><2>	70
clink_in<0>_d_p<0><2>	72
clink_in<0>_d_n<0><3>	76
clink_in<0>_d_p<0><3>	74
clink_in<0>_dck_n<0>	104
clink_in<0>_dck_p<0>	102
clink_in<0>_ser_rx_n	84
clink_in<0>_ser_rx_p	82
clink_out<0>_cc_n<0>	86
clink_out<0>_cc_p<0>	88
clink_out<0>_cc_n<1>	81
clink_out<0>_cc_p<1>	83
clink_out<0>_cc_n<2>	98
clink_out<0>_cc_p<2>	100
clink_out<0>_cc_n<3>	85
clink_out<0>_cc_p<3>	87
clink_out<0>_ser_tx_n	78
clink_out<0>_ser_tx_p	80

RS232

UCF name	Samtec pin	Description
rs232_in_invalid_l	97	Valid Signal Detector Output, Active Low. A logic-high indicates that a valid RS-232 level is present on a receiver input.
rs232_in_ready	22	Ready to Transmit Output, Active High.
rs232_in_rx	29	Receiver input to FPGA
rs232_out_force	105	Force-On, Active High. Drive high to override AutoShutdown of RS232 transceiver.
rs232_out_tx	99	Transmit output from FPGA.

RS232 Thru-hole header

Pin Number	Function
1	TX Output
2	Ground
3	RX Input

Electrical characteristics

The tables below show the electrical characteristics of the RS232 connection under typical operating conditions.

Receiver Inputs	Min	Typ	Max	Units
Input Voltage Range	-25		25	V
Input Threshold Low	0.6	1.2		V
Input Threshold High		1.5	2.4	V
Input Hysteresis		0.5		V
Input Resistance	3	5	7	kΩ

Transmitter Output	Min	Typ	Max	Units
Output Voltage Swing	±5	±5.4		V
Output Resistance	300	10M		Ω
Output Short-Circuit Current			±60	mA
Output Leakage Current			±25	µA

6. Marvell 88E1111 defaults

The Marvell 88E1111 is hardwired for the following configuration defaults:

PHYADR	"0001"
ENA_PAUSE	"0"
ANEG	"1111"
ENA_XC	"1"
DIS_125	"0"
HWCFG_MODE	"1111"
DIS_FC	"0"
DIS_SLEEP	"0"
SEL_TWSI	"0"
INT_POL	"1"
75/50 OHM	"0"

Revision History

Date	Revision	Nature of Change
Jul-2008	1.0	First release.
Oct-2008	1.1	Fixed mistakes in pin names, and added PHY defaults.
April-2008	2.0	Updated document to reflect hardware changes to the XRM-Clink-GIGE.