ALPHA DATA

ADC-VPX3-XMC
User Manual

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1 About the Hardware

The ADC-VPX3-XMC is an Open VPX compliant XMC carrier designed to host Alpha Data ADM-XRC series of FPGA mezzanine cards.

The ADC-VPX3-XMC is compatible with PCIe Gen2 and lower.

This carrier supports ADM-XRC series cards utilizing Virtex 6 and newer FPGAs.

Compliant with Vita 46.9 P2w1-P64s connections between P2 and XMC site J4.

Two full size mSATA sites offer massive SSD storage options.

Open VPX Compliance List

- SLT3-PAY-2F2U-14.2.3
- SLT3-PAY-1F1F2U-14.2.4
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-2F-14.2.7
- SLT3-PAY-1F4U-14.2.8
- SLT3-PAY-8U-14.2.9
- SLT3-PER-2F-14.3.1
- SLT3-PER-1F-14.3.2
- SLT3-PER-1U-14.3.3

1.1 Architecture

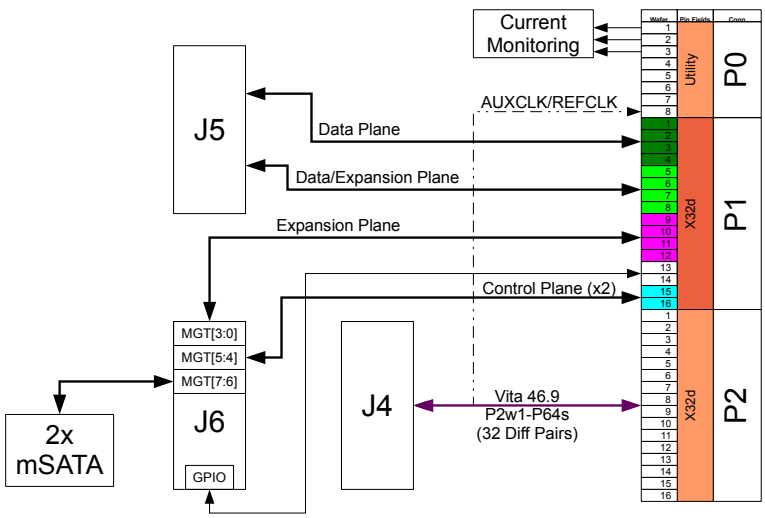

Figure 1 : ADC-VPX3-XMC Block Diagram

2 Board Features

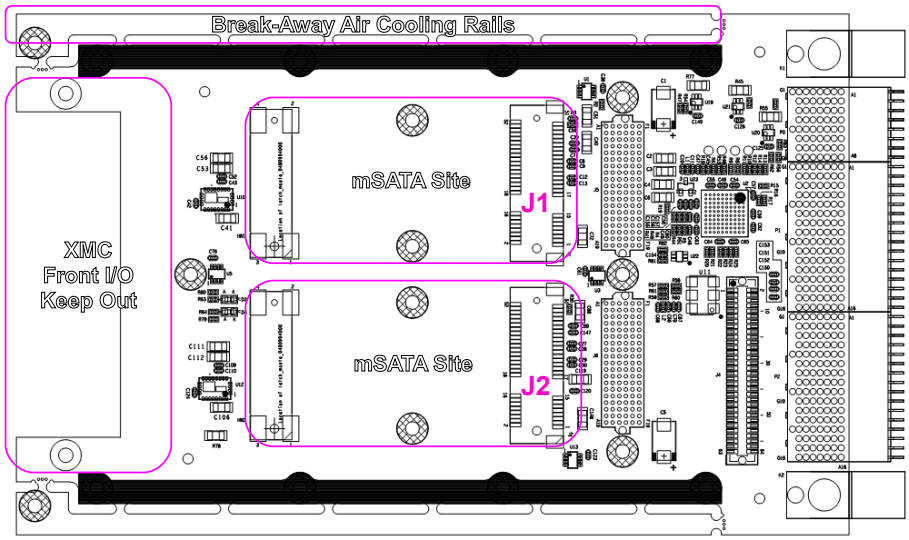

Figure 2 : Top Side Features

2.1 mSATA Sites

The ADC-VPX3-XMC can host two mSATA solid state drives. Access to these drives comes directly from the XMC processor card. Please see the Appendix for pin assignments. These mSATA devices are typically powered from the 3.3V supply rail only. However, if 1.5V is required for a particular mSATA device, a build option can be fitted to support this. Please contact sales@alpha-data.com for more details.

Optionally, the mSATA sites can be removed to allow more room for carrier metalwork for demanding conduction cooled applications. Please contact sales@alpha-data.com for more details.

The mSATA sites also support half length mSATA drives. However, special mounting hardware is required for this case.

2.2 Control Plane

The ADC-VPX3-XMC supports 2 Ultra-Thin Pipe control planes as per the OpenVPX standard. The control plane consists of two 1000Base-BX channels in the bottom two wafers of P1. Please see the Appendix for pin assignment information.

2.3 Clocking

2.3.1 PCIe REFCLK

An on-board PCIe REFCLK generator supplies the XMC site with the necessary 100MHz PCIe REFCLK.

2.3.2 AUXCLK

The ADC-VPX3-XMC forwards the AUXCLK signal from P0 through J4. This requires a change in resistor fit options and will consume part of the 46.9 P2w1-P64s configuration on VPX P2. Please see the Appendix for pin assignment details.

2.3.3 REFCLK

The ADC-VPX3-XMC forwards the REFCLK signal from P0 through J4. This requires a change in resistor fit options and will consume part of the 46.9 P2w1-P64s configuration on VPX P2. Please see the Appendix for pin assignment

2.4 System Controller

The ADC-VPX3-XMC supports the system controller feature of the VPX backplane. The SYSCON_L signal from P1 is fed into XMC ROOT0_L (making the XMC card the PCIe Arbiter).

When SYSCON_L is asserted, the XMC MRSTO_L will drive VPX_SYSRESET_L

2.5 Current Monitoring

The ADC-VPX3-XMC Provides current monitoring on the XMC input power rails (VPWR and 3.3V). Please contact Alpha Data at support@alpha-data.com for more details.

2.6 Cooling Option

The ADC-VPX3-XMC is designed to fully accommodate both air cooled and conduction cooled chassis both with and without front IO.

2.6.1 Air Cooled

Two removable tabs along the sides of board allow for easy insertion into standard air cooled chassis. Due to extremely low power consumption this carrier does not require any heatsinks in the air cooled configuration.

The removable tabs can be replaced by metal tabs if a customer requires a board that can be both air cooled and conduction cooled during its lifetime.

2.6.2 Conduction Cooled

A Vita 48.2 compliant conduction cooled frame will ship with the board for conduction cooled applications. All Alpha Data XMCs have conduction cooled options that are compliant with this carrier.

The heat frame for this board contains a removable front bar. With the front bar removed, Alpha Data front panel XRM modules can be used in conduction cooling application.

Custom conduction cooling assemblies can be designed to optimize heat transfer from critical components to the side rails as needed. Please contact sales@alpha-data.com for details.

2.7 VPX Mechanical Keying

The ADC-VPX3-XMC is delivered with the VPX guides unkeyed. For custom keying options please contact sales@alpha-data.com.

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Appendix A: Carrier Connector Pin Assignments

Signal	Carrier Connector.Pin	P0 Pin/Group
12V0	J5	Vs1
3V3	J5	Vs2
5V0	NA	Vs3
NVMRO	J5.C16	A4
VPX_SYSRESET_L	J5.F2	B4
M12V0_AUX	J5.F8	D4
TMS	J5.C6	B7
TDI	J5.C8	D7
TDO	J5.C10	E7
TCK	J5.C4	G7
AUXCLK_P	J4-25*	B8
AUXCLK_N	J4-27*	C8
REFCLK_P	J4-46*	E8
REFCLK_N	J4-48*	F8

Table 1 : P0 Pin Assignments

* Requires build option.

Signal	Carrier Connector.Pin	Carrier Connector.Pin
SATA1_TX_P	J6.A7	J1.33
SATA1_TX_N	J6.B7	J1.31
SATA1_RX_P	J6.A17	J1.23
SATA1_RX_N	J6.B17	J1.25
SATA2_TX_P	J6.D7	J2.33
SATA2_TX_N	J6.E7	J2.31
SATA2_RX_P	J6.D17	J2.23
SATA2_RX_N	J6.E17	J2.25

Table 2 : mSATA Pin Assignments

Signal	Carrier Connector.Pin	P1 Pin		P1 Pin	Carrier Connector.Pin	Signal
SYSCON_L	J5.E19	G5	|	-	-	-
PCIE_RX0_P	J5.A11	A1	|	A9	J6.A11	J6_RX0_P
PCIE_RX0_N	J5.B11	B1	|	B9	J6.B11	J6_RX0_N
PCIE_TX0_P	J5.A1	D1	|	D9	J6.A1	J6_TX0_P
PCIE_TX0_N	J5.B1	E1	|	E9	J6.B1	J6_TX0_N
PCIE_RX1_P	J5.D11	B2	|	B10	J6.D11	J6_RX1_P
PCIE_RX1_N	J5.E11	C2	|	C10	J6.E11	J6_RX1_N
PCIE_TX1_P	J5.D1	E2	|	E10	J6.D1	J6_TX1_P
PCIE_TX1_N	J5.E1	F2	|	F10	J6.E1	J6_TX1_N
PCIE_RX2_P	J5.A13	A3	|	A11	J6.A13	J6_RX2_P
PCIE_RX2_N	J5.B13	B3	|	B11	J6.B13	J6_RX2_N
PCIE_TX2_P	J5.A3	D3	|	D11	J6.A3	J6_TX2_P
PCIE_TX2_N	J5.B3	E3	|	E11	J6.B3	J6_TX2_N
PCIE_RX3_P	J5.D13	B4	|	B12	J6.D13	J6_RX3_P
PCIE_RX3_N	J5.E13	C4	|	C12	J6.E13	J6_RX3_N
PCIE_TX3_P	J5.D3	E4	|	E12	J6.D3	J6_TX3_P
PCIE_TX3_N	J5.E3	F4	|	F12	J6.E3	J6_TX3_N
PCIE_RX4_P	J5.A15	A5	|	A13	J6.F13	GP14
PCIE_RX4_N	J5.B15	B5	|	B13	J6.F12	GP16
PCIE_TX4_P	J5.A5	D5	|	D13	J6.C13	GP13
PCIE_TX4_N	J5.B5	E5	|	E13	J6.C12	GP15
PCIE_RX5_P	J5.D15	B6	|	B14	J6.F15	GP10
PCIE_RX5_N	J5.E15	C6	|	C14	J6.F14	GP12
PCIE_TX5_P	J5.D5	E6	|	E14	J6.C15	GP9
PCIE_TX5_N	J5.E5	F6	|	F14	J6.C14	GP11
PCIE_RX6_P	J5.A17	A7	|	A15	J6.A15	ETH2_RX_P
PCIE_RX6_N	J5.B17	B7	|	B15	J6.B15	ETH2_RX_N
PCIE_TX6_P	J5.A7	D7	|	D15	J6.A5	ETH2_TX_P
PCIE_TX6_N	J5.B7	E7	|	E15	J6.B5	ETH2_TX_N
PCIE_RX7_P	J5.D17	B8	|	B16	J6.D15	ETH1_RX_P
PCIE_RX7_N	J5.E17	C8	|	C16	J6.E15	ETH1_RX_N
PCIE_TX7_P	J5.D7	E8	|	E16	J6.D5	ETH1_TX_P
PCIE_TX7_N	J5.E7	F8	|	F16	J6.E5	ETH1_TX_N

Table 3 : P1 Pin Assignments

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	J6.C19	GND	Jn4-1	Jn4-3	GND	Jn4-2	Jn4-4
2	GND	Jn4-5	Jn4-7	GND	Jn4-6	Jn4-8	GND
3	J6.F19	GND	Jn4-9	Jn4-11	GND	Jn4-10	Jn4-12
4	GND	Jn4-13	Jn4-15	GND	Jn4-14	Jn4-16	GND
5	J6.C18	GND	Jn4-17	Jn4-19	GND	Jn4-18	Jn4-20
6	GND	Jn4-21	Jn4-23	GND	Jn4-22	Jn4-24	GND
7	J6.F18	GND	Jn4-25	Jn4-27	GND	Jn4-26	Jn4-28
8	GND	Jn4-29	Jn4-31	GND	Jn4-30	Jn4-32	GND
9	J6.C17	GND	Jn4-33	Jn4-35	GND	Jn4-34	Jn4-36
10	GND	Jn4-37	Jn4-39	GND	Jn4-38	Jn4-40	GND
11	J6.F17	GND	Jn4-41	Jn4-43	GND	Jn4-42	Jn4-44
12	GND	Jn4-45	Jn4-47	GND	Jn4-46	Jn4-48	GND
13	J6.C16	GND	Jn4-49	Jn4-51	GND	Jn4-50	Jn4-52
14	GND	Jn4-53	Jn4-55	GND	Jn4-54	Jn4-56	GND
15	J6.F16	GND	Jn4-57	Jn4-59	GND	Jn4-58	Jn4-60
16	GND	Jn4-61	Jn4-63	GND	Jn4-62	Jn4-64	GND

Table 4 : P2 Pin Assignments

Revision History

Date	Revision	Changed By	Nature of Change
25 Sep 2012	0.1	K. Roth	Preliminary
14 Jan 2013	0.2	K. Roth	Fixed typos and updated images.
16 Apr 2014	2.0	K. Roth	Updated entire design specification to match rev2 PCB.
1 Oct 2015	2.1	K. Roth	Corrected P1 pin assignment table errors.
22 Jan 2016	2.2	K. Roth	Updated Top Side Features to clearly show mSATA site labels.
10 May 2018	2.3	K. Roth	Updated P2 Pin Assignments to correct error in pin number of all column G signals.

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